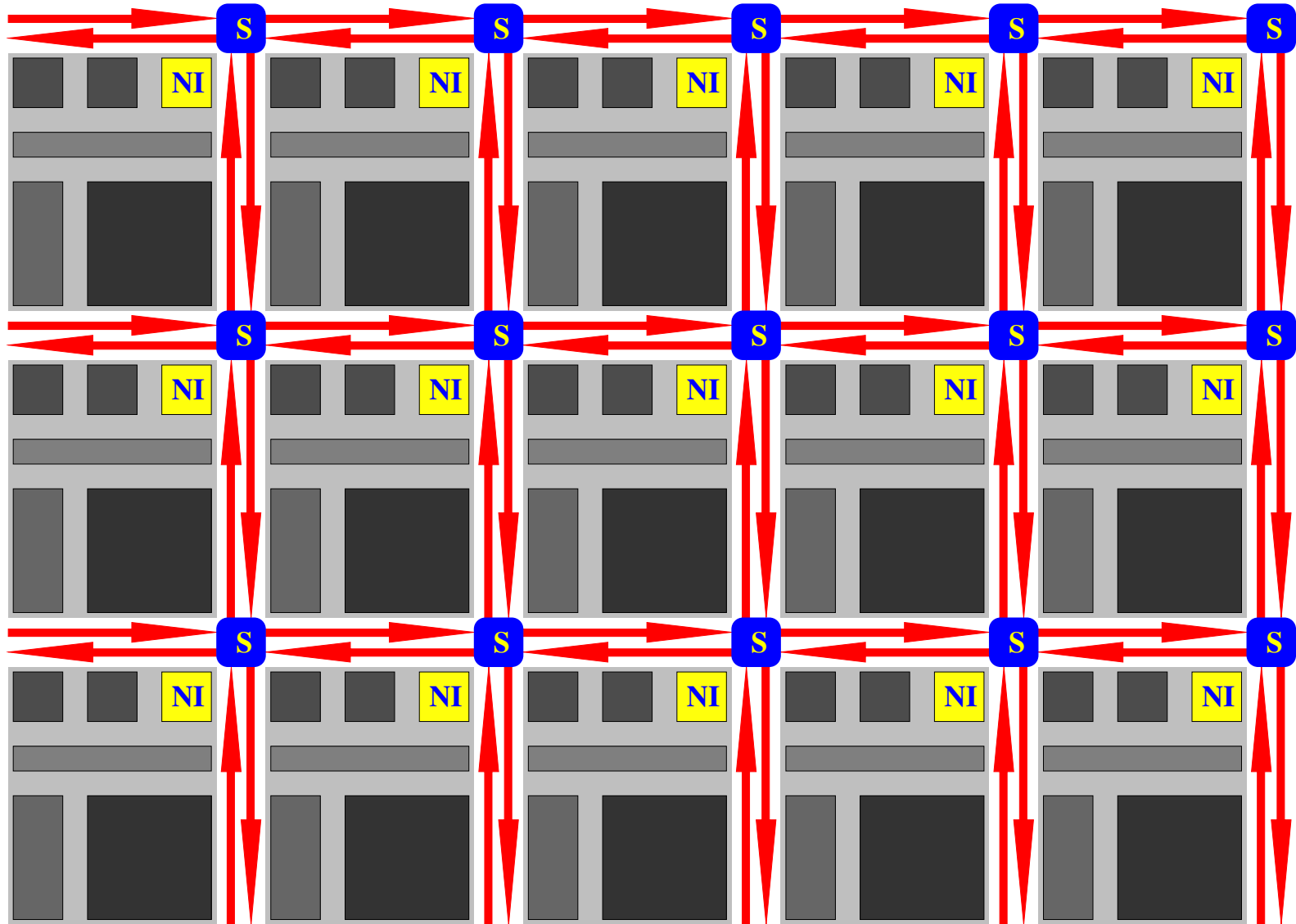


# **Power Analysis of Link Level and End-to-end Protection in Networks on Chip**

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Royal Institute of Technology, Stockholm

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# Overview

Assumptions

Experimental Setup

Link Level Low Power Encoding

Link Level Data Protection

End-to-end Data Protection

Conclusion



## Boundary Conditions and Assumptions

- Nostrum NoC:
  - ★ Deflective routing with no internal buffers
  - ★  $2 \times 128$  bit 2mm switch to switch links



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- We consider faults on long wires only



# Link Level Low Power Encoding

- Requirements:
  - ★ Low area overhead
  - ★ Fast and short critical path
  - ★ Low power consumption
- Configuration A: Reference configuration with no low power encoding
- Configuration B: Bus invert encoding (P1BI)
- Configuration C: 2 partition bus invert encoding (P2BI)



## Delay and Clock Period for Link Level Encoding

Conf.	Block	delay [ns]	total delay	frequency
A	Switch	$0.42ns$	0.42 ns	2.38 GHz
	Link	$0.08ns$		
B	Switch	$0.42ns$	2.52 ns	0.39 GHz
	Enc.	$2.43ns$		
	Dec.	$0.01ns$		
	Link	$0.08ns$		
C	Switch	$0.42ns$	1.37 ns	0.73 GHz
	Enc.	$1.28ns$		
	Dec.	$0.01ns$		
	Link	$0.08ns$		



## Power Consumption Normalized with Respect to Performance

Conf.	$V_{dd}$	Block	Switching activity %	Power consumption [mW]
A	0.51	Switch	20.8	2.26
		4 links	20.8	281.23
		Total		283.49
B	0.90	Switch	20.8	7.03
		4 Enc.	20.8	7.98
		4 Dec	19.6	0.86
		4 links	19.6	826.99
		Total		842.86
C	0.70	Switch	20.8	4.26
		4 Enc.	20.8	3.81
		4 Dec	19.0	0.49
		4 links	19.0	484.28
		Total		492.84



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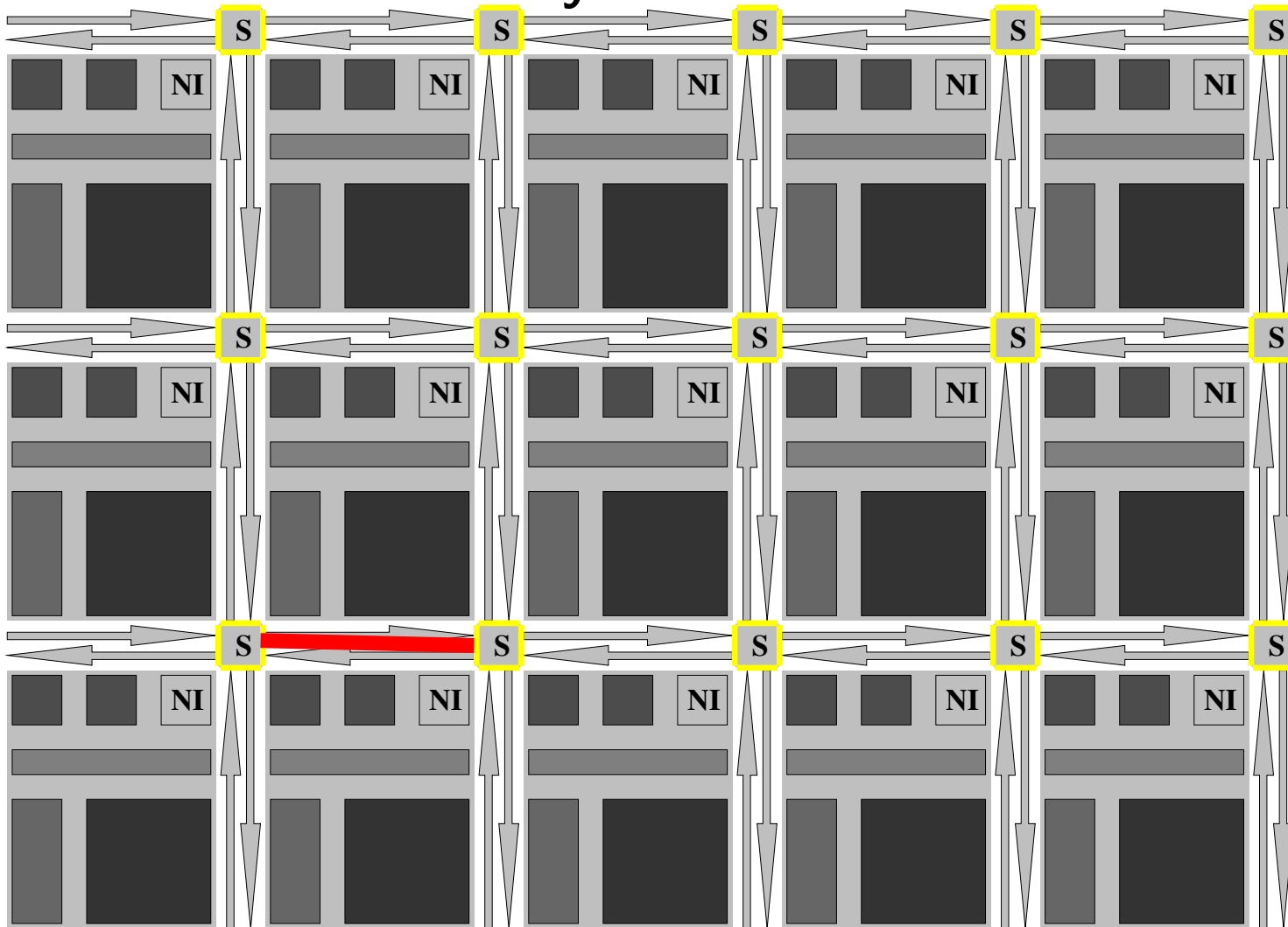


# Error Protection for Low Power Communication

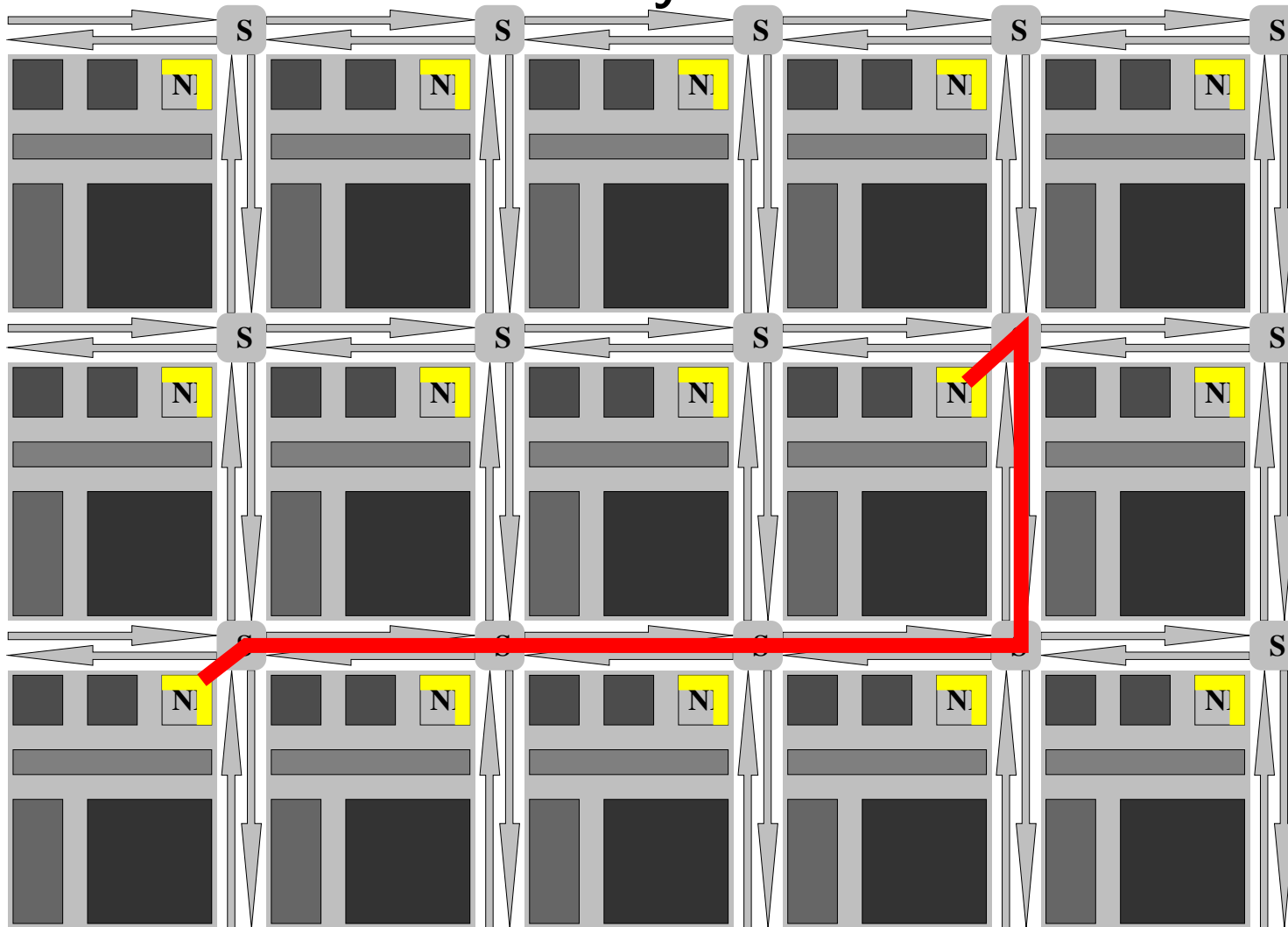
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  - ★ Scenario III: Network level (end-to-end) error protection



# Link Layer Protection



# End-to-end Layer Protection



## Error Protection for Low Power

### Scenario I:

- $8 \times 8$  network
- 80 bits payload
- 15 bits header

### Scenario II: Link layer error protection

- Block code with DED/SEC capability
- 20 payload bits and 5 protection bits per block;
- 80 payload bits
- 15 header bits
- 30 protecting bits
- 125 total bits

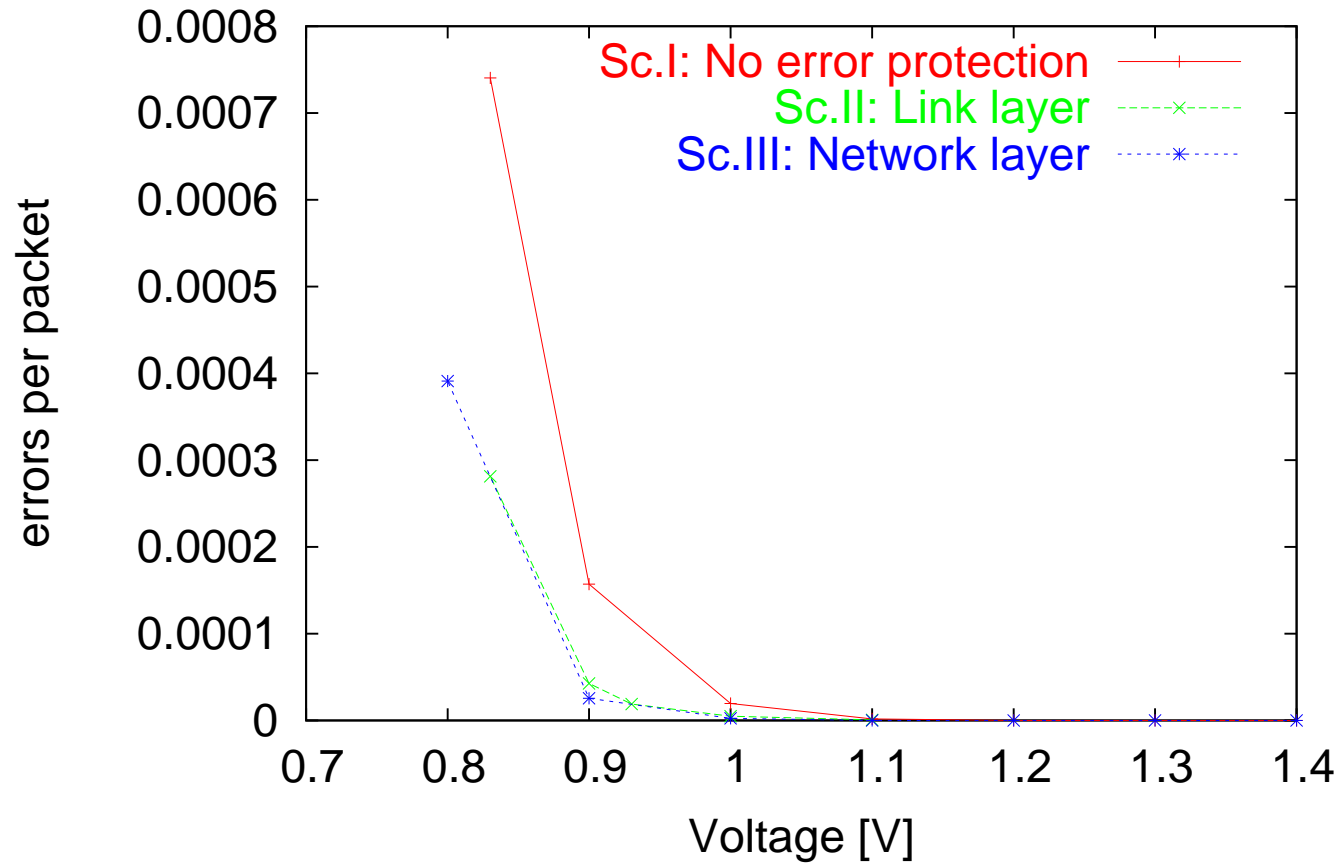
### Scenario III: End-to-end protection

- Header is protected at the link layer as in Scenario II
- Payload is protected by a block code with SEC/DED capability
- 80 payload bits
- 15 header bits
- 24 protecting bits
- 119 total bits



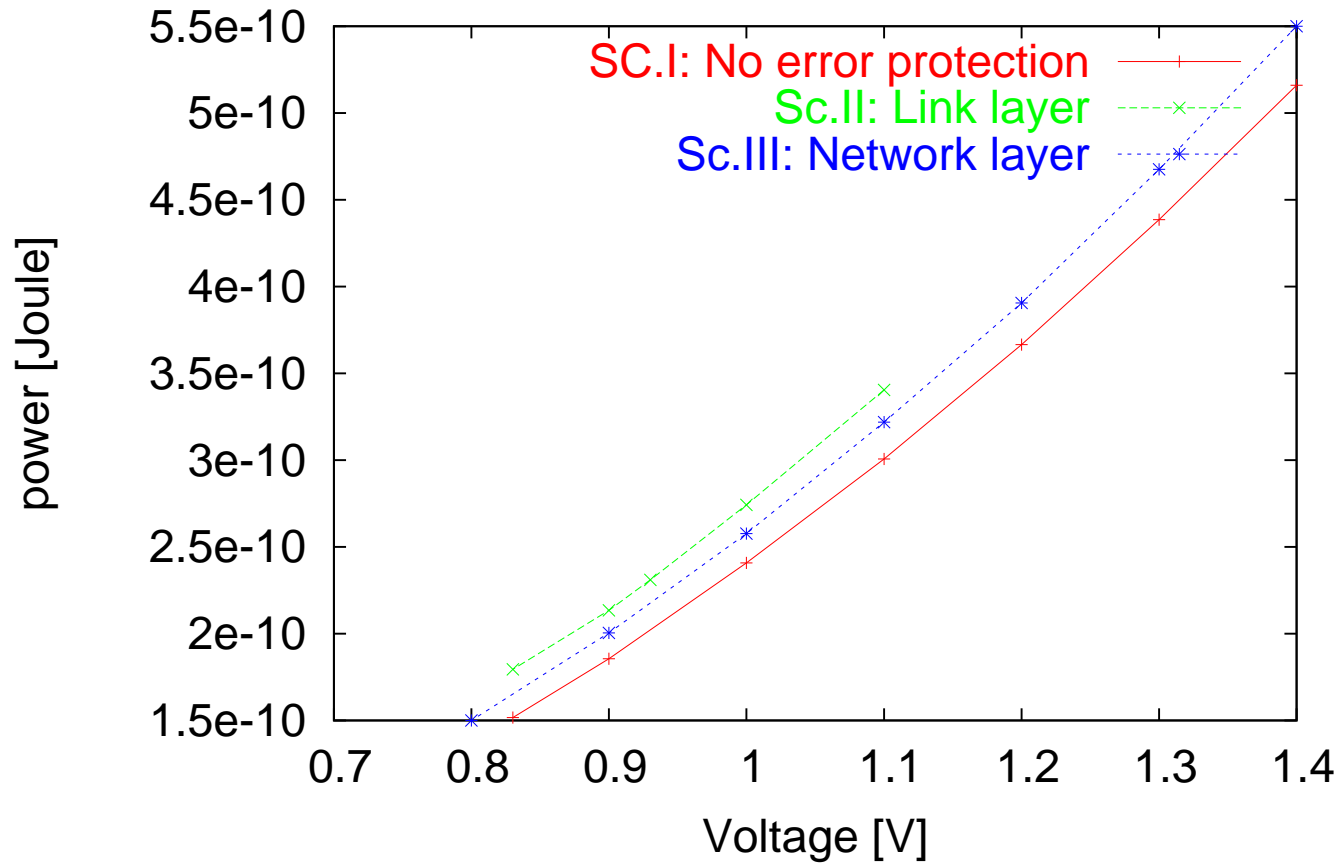
# Errors per Packet

Errors per packet depending on the voltage



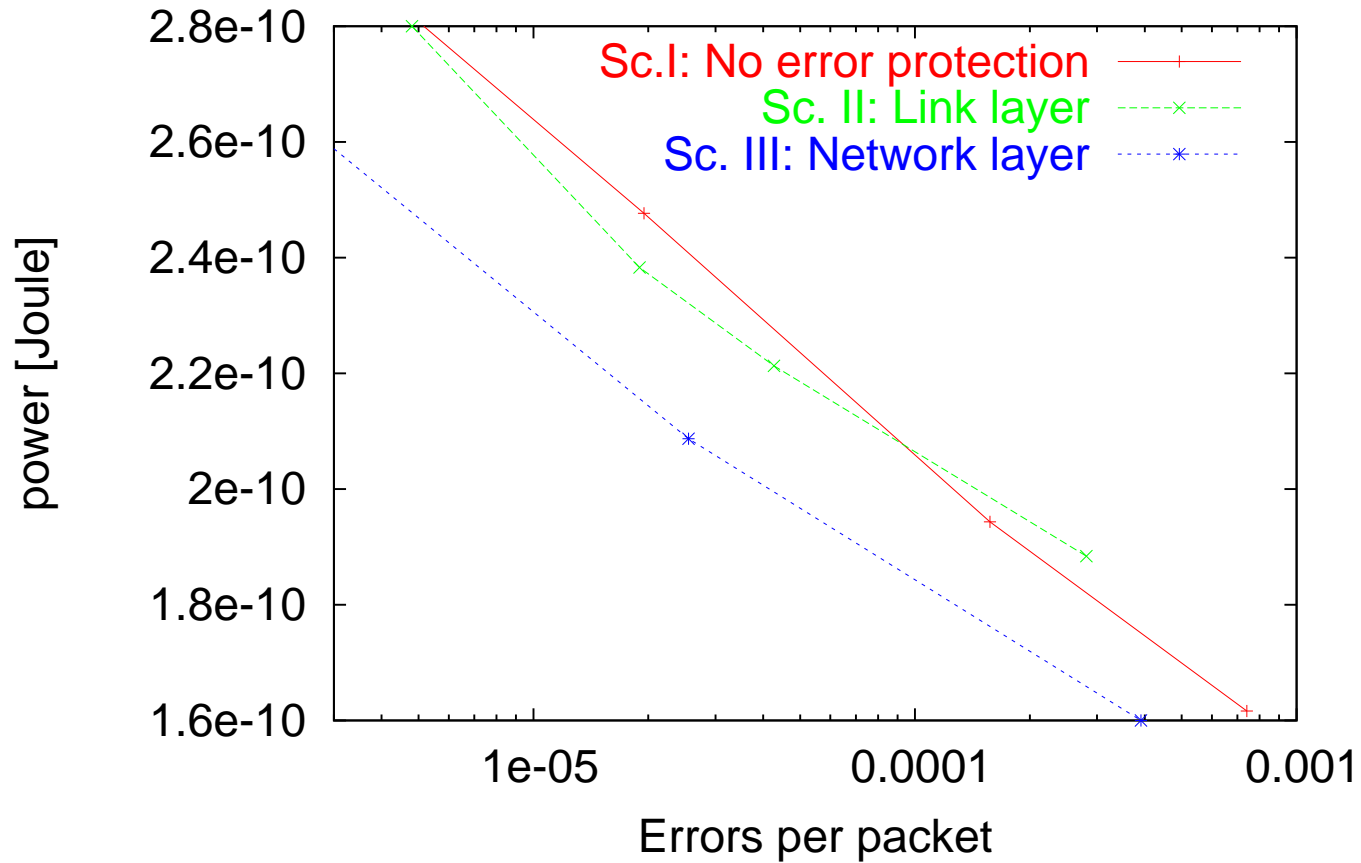
# Power Consumption per Useful Bit

Power consumption per useful bit depending on the voltage



# Power Consumption vs. Error Rate

power consumption vs error rate



## Conclusion

- Low power bus encoding is of limited value and probably increases the overall power consumption.
- Link-level error protection to allow for lower voltage does not give significant improvements.
- End-to-end data protection decreases power consumption for  $8 \times 8$  networks, with slowly increasing gain for larger networks.

