

Curriculum Vitae

Axel Jantsch
February 2010

1. Personal facts

- Full name: Axel Arthur Jantsch
- born in Klagenfurt, Austria, on December 20, 1962.
- Married since April 1988; 2 children.
- Current position:
Professor in Electronic System Design at the
Department of Electronics, Computer and Software Systems,
School of Information and Communication Technology
Royal Institute of Technology,
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Home page: www.web.it.kth.se/~axel

2. Languages

- Fluent in German, English and Swedish.

3. Education

- January 1988: Dipl.Ing. in Informatik (Master), Technical University Vienna, Title of thesis: *Probleme der Morphologie bei sprachanalyisierenden Systemen (Morphological Problems in Language Analysing Systems)*.
- December 1992: Dr. Tech. in Computer Science (PhD), Technical University Vienna, Title of thesis: *Design Space Exploration with Estimation Functions and Design Style Description*.
- June 2000: Docent of the Royal Institute of Technology, title of docent lecture: "Electronic Design Automation: The next 50 Years".

4. Research Interests:

- Embedded systems
- Networks on Chip
- VLSI and SoC Design
- HW/SW Codesign
- Modelling concepts and languages
- Design methodology
- System synthesis and validation

5. Professional Positions and Employment:

- 1983 - 1988: Development of financial software and accounting systems as part time employment at Schellenberger GmbH, Vienna.
- March 1988 - February 1993: Research and teaching assistant at Institut für Technische Informatik, Technical University Vienna.
- April 1993 - March 1995: Guest researcher at Electronic Systems Design Lab, Royal Institute of Technology, Stockholm, Sweden, financed by a Schrödinger grant of the Austrian Science Foundation.
- June 1995 - December 1996: employed by Siemens Austria AG in Vienna.
- since January 1997: Univ lektor (Associate Professor) at Department of Electronics, Royal Institute of Technology (KTH), Stockholm, Sweden.
- January 1999 - December 2002: Program manager of the Foundation for Strategic Research (SSF) funded national research program Integrated Electronic Systems (INTELECT), with a duration of four years and a budget of SEK 110 million.
- since December 2002: Full professor in Electronic System Design at KTH
- January 2004 – October 2005: Head of LECS laboratory (8 professors, 65 persons)
- Since September 2005: Member of the Steering Group at FrameAccess AB
- Since October 2006: Responsible director for the international Master Program System on Chip Design”
- March 2007-June 2007: Guest Professor at University of Technology Vienna, Vienna, Austria
- December 2007: Guest Professor at Fudan University, Shanghai, China
- January 2009: Guest Professor at University of Cantabria, Santander, Spain
- June 2009: Guest Professor at Fudan University, Shanghai, China
- Since July 2009 Head of Unit Electronic Systems (60 persons)

6. Experience in Education

6.1 Lab assistant and occasional lectures

- Computer Architecture, 3rd year, TU Vienna, 1988
- VLSI Design, 5th year, TU Vienna, 1988
- Computer Architecture, 3rd year, TU Vienna, 1989
- VLSI Design, 5th year, TU Vienna, 1989
- Computer Architecture, 3rd year, TU Vienna, 1990
- VLSI Design, 5th year, TU Vienna, 1990
- Computer Architecture, 3rd year, TU Vienna, 1991
- Computer Architecture, 3rd year, TU Vienna, 1992

6.2 Invited Course Lectures

- NorESD Seminar Series, lectures on *HW/SW Cosimulation*, Stockholm, Sweden, April 1993.

- NorESD Seminar series, lectures on *HW/SW Codesign and Performance Estimation*, Stockholm, Sweden, April 1994.
- HW/SW Codesign, Graduate Course, Linköping University, Sweden, 1998, lecture on *Concurrent Engineering*.
- Embedded Systems course, 4th year, in Jönköping University, Sweden, February 2000, lecture series on *System Methodologies*.
- Embedded Systems course, 4th year, in Jönköping University, Sweden, March 2000, lecture series on *System Modelling and Specification*.
- Datorsystem, 4th year, in Mithögskolan Sundsvall, Sweden, April 2000, lecture on *System Modelling and Specification*.
- System on Chip Eurotraining Course, Grenoble, France, May 2000, lecture on *Models of Computation*.
- System on Chip Eurotraining Course, Lyngby, Denmark, November 2000, lecture on *Models of Computation*.
- System on Chip Eurotraining Course, Stockholm, Sweden, May 2001, lecture on *Models of Computation*.
- Embedded Systems Course in SOC Master Program, Royal Institute of Technology, Stockholm, Sweden, October 2000, lecture on *Microprocessor Architectures*.
- Embedded Systems Course in SOC Master Program, KTH, October 2000, lecture on *Compiler Techniques*.
- Embedded Systems Course in SOC Master Program, KTH, October 2000, lecture on *Hardware Acceleration*.
- Embedded Systems Course in SOC Master Program, KTH, October 2000, lecture on *Networks*.
- SoC Architecture Course in SOC Master Program, KTH, December 2002, lecture on *Networks on Chip*
- *Will networks on chip close the productivity gap?* Presentation at the Special Topics in SoC Course at KTH, May 2003.
- *Network on Chip Tutorial*. Invited lecture at the Stringent Summer School, August 2003, Örebro, Sweden.
- *Networks on Chip*. Invited tutorial at the IEEE NorCHIP Conference, Riga, Latvia, November 2003.
- *Performance in Networks on Chip*. Guest lecture in SoC Architecture course at KTH, November 2003.
- *Networks on chip*. Invited seminar at Linköping University, November 2004.
- *Communication performance in network-on-chips*. Short course at Tallinn Technical University, October 2006.
- *Exchange of course modules across Universities*. Invited presentation at the 6th European Workshop on Microelectronic Education, June 2006.
- Tiberius Seceleanu, Axel Jantsch, and Hannu Tenhunen. *On-chip distributed architectures*. Tutorial at the International SoC Conference, September 2006. Austin, Texas.
- Axel Jantsch, Luca Benini, Timothy M. Pinkston, Kees Goossens, Pieter van der Wolf, Alian Fanet and Marcello Coppola, *NoC at the Age of Six: Advanced Topics, Current*

Challenges and Trends, tutorial at Design Automation and Test Europe Conference, DATE 2007, Nice, France.

- Axel Jantsch, Luca Benini and Radu Marculescu, *Networks on Chip*, Tutorial at the First International Network on Chip Symposium, May 2007, Princeton, USA.
- Axel Jantsch and Dave Gwilt, *Network on Chip*, Tutorial at Asian and South Pacific Design Automation Conference, ASP-DAC, January 2008, Seoul, South Korea.
- Eugenio Villar, Axel Jantsch, Christoph Grimm and Tim Kogel, *Heterogeneous System Level Specification using SystemC*, Tutorial at the Design Automation and Test Europe Conference, DATE 2008, Munich, Germany.
- Axel Jantsch and Zhonghai Lu. Quality of service in networks on chip. Invited Seminar at the Research Center Telecommunication Vienna (FTW), April 2008.
- Axel Jantsch. Nostrum network on chip. Invited Seminar at the Turku center of Computer Science, April 2008.
- Axel Jantsch. Resource allocation for quality of service on-chip communication. Invited seminar at the real Time Research Center in Vasteras, Sweden, February 2009.
- Axel Jantsch. Resource allocation for quality of service on-chip communication. Invited seminar at the University of Cantabria, Santander, Spain, February 2009.
- Axel Jantsch and Zhonghai Lu. Networks on chip. Short course at Fudan University, June 2009.
- Axel Jantsch et al. The Nostrum network on chip. Invited Seminar at Fudan University, June 2009.
- Axel Jantsch and Zhonghai Lu. Trends in terascale on-chip computing 2010-2020. Invited Seminar at Nanjing University, July 2009.
- Axel Jantsch and Zhonghai Lu. Trends in terascale on-chip computing 2010-2020. Invited Seminar at the ICES annual conference, September 2009.
- Zhonghai Lu and Axel Jantsch. Trends in of terascale computing chips in the next ten years. Invited talk at *IEEE ASICON 2009*, ChangSha, China, October 2009.

6.3 Course responsible

- Silicon Compilation, 5th year, TU Vienna, Austria, 1990, 1991, 1992
- Concurrent Engineering, 4th year, Royal Institute of Technology, 1995, 1996, 1997, 1998, 1999, 2000.
- Advanced Topics in System Synthesis, Graduate Course, Royal Institute of Technology, 1999-2003, 2006.
- System Modelling, 4th year, Royal Institute of Technology, 2001, 2002, 2003, 2004, 2005, 2006, 2007, 2008. This course is given for the E section students, for the IT-University students and for the Master program in System-on-Chip.
- Advanced Topics in System Modelling, Graduate Course, KTH, 2001-2003.
- Embedded Systems, 4th year, Royal Institute of Technology, 2001, 2002; This course is given for the E section students, for the IT-University students and for the Master program in System-on-Chip students.
- System Modelling. A SoC-Mobinet course given at Denmark Technical University, Lyngby, Denmark, February-May 2004.

- System Modeling. A distance learning course offered to small and medium enterprises in the five nordic and three Baltic countries as part of the SoC-SME project, January-September 2004.
- System Modeling. Guest lecturer at University of Technology Vienna, Austria, March 2007 – June 2007.
- System on Chip Architecture. Full course given in December 2007 – January 2008 at Fudan University, Shanghai, China.
- SoC Design Project Course for SoC Design students; 2007, 2008.
- SoC Architecture at KTH; 2008, 2009, 2010.

6.4 Master thesis supervision

1990-1997

1. Wolfgang Stubenvoll, *Vorbereitende Arbeiten zur Herstellung des Mandelbrotchips*, Vienna, 1990.
2. Alexander Jenewein, *Architekturentwurf zur Herstellung des Mandelbrotchips unter Genesil*, Vienna, 1991.
3. Adam Martony, *A Cross Compiler Prototype for the Digital Signal Processor TMS320C5x*, masters thesis, Royal Institute of Technology, Sweden, TRITA-ESD-1995-11, 1995.
4. Johann Notbauer, *Testfall und Testfallumgebung: Spezifikation in VHDL basierend auf Ereignissen und Zuständen*, masters thesis, Technische Universität Graz, Austria, 1996.
5. Fredrik Hoffman. *VHDL design and implementation analysis of an embedded controller*. Master's thesis, Royal Institute of Technology, Stockholm, Sweden, 1997, ISRN KTH/ESD/R-97/15-SE.
6. Wolfgang Horn, *Modelling of an ATM Multiplexer in a Network Terminal for a Mixed Hardware/Software Implementation*, masters thesis, Technische Universität Graz, Austria, 1998.

1998

7. Björn Molin, *Evaluation of a Retargetable DSP-C Compiler*, masters thesis, Royal Institute of Technology, Sweden, December 1998.
8. Heiko Hubert. *A survey of HW/SW cosimulation techniques and tools*. Master's thesis, Royal Institute of Technology, Stockholm, Sweden, 1998, TRITA-ESD-1998-07.

1999

9. Yuxin Guo. *A test system for an access point in wireless LAN*. Master's thesis, Kungliga Tekniska Högskolan, Stockholm Sweden, November 1999. ELE/ESD/1999-6.

2000

10. Johan M. Ditmar. *A dynamically reconfigurable FPGA-based content addressable*

memory for IP characterization. Master's thesis, Kungliga Tekniska Högskolan, Stockholm, Sweden, March 2000.

11. Emil Sävqvist. *Hardware fault insertion techniques and tools*. Master's thesis, Kungliga Tekniska Högskolan, Stockholm, Sweden, February 2000.
12. Robert Thorhuus. *Software fault injection testing*. Master's thesis, Kungliga Tekniska Högskolan, Stockholm, Sweden, February 2000.

2001

13. Anders Agner and Lars Rådvall, *Simulation and Evaluation of Multicast Implementations in a Packet Switch*, masters thesis, Department of Microelectronics and Information Technology, Royal Institute of Technology, Stockholm, Sweden, ELE/ESK/2001-13, September 2001.
14. Arnaud Ferre Ciuro, *ClearSyDe: A Graphical User Interface for the ForSyDe Methodology*, masters thesis, Department of Microelectronics and Information Technology, Royal Institute of Technology, Stockholm, Sweden, ELE/ESK/2001-14, October 2001.
15. Fredrik Claesson, *Fingerprint Identification using Mathematical Morphology*, masters thesis, Department of Electronics, Royal Institute of Technology, Stockholm, Sweden, Electrum 229, S-16440 Kista, Sweden, ELE/ESK/2000-4, March 2001.
16. Shirley Cui, *Behavioural Modelling of the Bluetooth Baseband Protocol*, masters thesis, Department of Microelectronics and Information technology, Royal Institute of Technology, Stockholm, Sweden, ELE/IMIT/2001-16, December 2001.
17. Zhonghai Lu, *Refinement of a System Specification for a Digital Equalizer into HW and SW Implementations*, Department of Microelectronics and Information Technology, Royal Institute of Technology, masters thesis, IMIT/2001-18, December 2001.
18. Yi-Ran Sun, *Simulation and Performance Evaluation for Networks on Chip*, masters thesis, Department of Microelectronics and Information Technology, Royal Institute of Technology, Stockholm, Sweden, ELE/IMIT/2001-17, December 2001.

2002

19. Rikard Thid, *A Network on Chip Simulator*, masters thesis, Department of Microelectronics and Information Technology, Royal Institute of Technology, IMIT/LECS 2002-17, August 2002.
20. Erland Nilsson, *Design and Implementation of a Hot-potato Switch in a Network on Chip*, masters thesis, Department of Microelectronics and Information Technology, Royal Institute of Technology, IMIT/LECS 2002-11, Stockholm, Sweden, June 2002.
21. Heiko Zimmer, *Fault Modelling and Error-Control Coding in a Network-on-Chip*, masters thesis, Laboratory of Electronics and Computer Systems, Royal Institute of Technology (KTH), Stockholm, IMIT/LECS 2002-26, 2002.
22. Ningning Zhang, *Performance Estimation in ForSyDe*, masters thesis, Institute of Microelectronics and Information Technology, Royal Institute of Technology (KTH), Stockholm, Sweden, IMIT/LECS/2002-25, December 2002.
23. Hua Tian, *Refinement in ForSyDe*, masters thesis, Institute of Microelectronics and Information Technology, Royal Institute of Technology (KTH), Stockholm, Sweden, IMIT/LECS/2002-23, December 2002.

2003

24. Johan Karlsson, *DSP System Design Using MASIC Methodology: A Case Study*, masters thesis, Laboratory of Electronics and Computer Systems, Royal Institute of Technology (KTH), Stockholm, IMIT-LECS/2003-02, March 2003.
25. Lars Strid, *Traffic Loops for ATM Termination Boards*, masters thesis, Laboratory of Electronics and Computer Systems, Royal Institute of Technology (KTH), Stockholm, IMIT-LECS/2003-03, March 2003.
26. Adelina Shickova, *Architecture Exploration of Interconnection Networks as a Communication Layer for Reconfigurable Systems*, masters thesis, Institute of Microelectronics and Information Technology, Royal Institute of Technology (KTH), Stockholm, Sweden, IMIT-LECS 2003-38, September 2003.
27. Paulius Dambrauskas, *Real-time Guitar Chord Recognition*, masters thesis, Institute of Microelectronics and Information Technology, Royal Institute of Technology (KTH), June 2003.
28. Björn Bertilsson and Sebastian Ritter, *W-CDMA Receiver Model for Network-on-Chip*, masters thesis, Institute of Microelectronics and Information Technology, Royal Institute of Technology (KTH), 2003.
29. Andrei Arakelov, *Segmented Bus Structures in Globally-Asynchronous Locally-Synchronous System-on-Chip Designs*, masters thesis, Institute of Microelectronics and Information Technology, Royal Institute of Technology (KTH), June 2003.

2004

30. Andreas Källkvist and Tobias Zetterlund, *Evaluation of Rational Rose in a Real-time Environment*, masters thesis, Institute of Microelectronics and Information Technology, Royal Institute of Technology (KTH), Stockholm, Sweden, IMIT-LECS 2004-1, March 2004.
31. Dmitry Shipilov, *Design and Implementation of the Resource-Network Interface for Networks-on-Chip*, masters thesis, Institute of Microelectronics and Information Technology, Royal Institute of Technology (KTH), Nostrum, Stockholm, Sweden, June 2004.
32. Juan Mata Pavia, *Design and Implementation of a Fat Tree Network on Chip*, masters thesis, Institute of Microelectronics and Information Technology, Royal Institute of Technology (KTH), Nostrum, Stockholm, Sweden, June 2004.
33. Arseni Vitkowski, *A Study on Power Consumption in the Nostrum Communication Network*, masters thesis, Institute of Microelectronics and Information Technology, Royal Institute of Technology (KTH), Nostrum, Stockholm, Sweden, April 2004.
34. Farhadur Arifin, *Implementation and Evaluation of Segmented-Bus Architecture*, masters thesis, Institute of Microelectronics and Information Technology, Royal Institute of Technology (KTH), December 2004.
35. Sebastian Jäger, *Technical and Economical Barriers and Drivers for the Introduction of Formal Methods in the Verification of Digital Systems*, masters thesis, Darmstadt University of Technology, Department of Electrical Engineering and Information Technology, January 2004.

2005

36. Tong Li, *Estimation of Power Consumption in Wormhole Routed Networks on Chip*,

- masters thesis, Institute of Microelectronics and Information Technology, Royal Institute of Technology (KTH), Nostrum, April 2005.
37. Karl-Henrik Nielsen, Evaluation of Real-time Performance Models in Wormhole-routed On-chip Networks, masters thesis, Institute of Microelectronics and Information Technology, Royal Institute of Technology (KTH), Nostrum, Stockholm, Sweden, April 2005.
 38. Jonas Sicking, Implementation of asynchronous communication for ForSyDe in hardware and software, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, ForSyDe, Stockholm, Sweden, December 2005.
 39. Marek Andrzejewski, AMBA Bus Emulation in the Nostrum NoC using Best Effort Communication, masters thesis, School for Information and Communication Technology, Nostrum, Stockholm, Sweden, December 2005.
 40. Daniel Åkerlund, Implementation of a 2x2 NoC with Wishbone Interface, masters thesis, School for Information and Communication Technology, Nostrum, Stockholm, Sweden, November 2005.
 41. Sandro Penolazzi, An Empirical Power Model of the Links and the Deflective Routing Switch in Nostrum, masters thesis, School for Information and Communication Technology, Nostrum, Stockholm, Sweden, December 2005.
 42. Smaran Kanti Paul, Development of a Power Modeling and Estimation Technique within a Power aware Design Methodology, masters thesis, School for Information and Communication Technology, Stockholm, Sweden, December 2005.
 43. Ming Liu, Improving the Performance of a Wormhole Router and Wormhole Flow Control, masters thesis, School for Information and Communication Technology, Nostrum, Stockholm, Sweden, December 2005.
 44. Guang Liang, Design of Frequency Controller for Minimizing Power Consumption In Network-on-Chip, masters thesis, School for Information and Communication Technology, Nostrum, Stockholm, Sweden, October 2005.
 45. Mingchen Zhong, Evaluation of Deflection-routed On-Chip Networks, masters thesis, School for Information and Communication Technology, Nostrum, Stockholm, Sweden, August 2005.
 46. Xian Qian, Implementation of a JPEG Encoder on the Nostrum Network-on-Chip, masters thesis, School for Information and Communication Technology, Nostrum, Stockholm, Sweden, July 2005.
 47. Bjarke Thormann, Modeling of Dynamic Resource Allocation in a Network on Chip, masters thesis, School for Information and Communication Technology, Nostrum, Stockholm, Sweden, June 2005.
 48. Bei Yin, Design and Implementation of a Wormhole Router Supporting Multicast for Networks on Chips, masters thesis, Institute of Microelectronics and Information Technology, Nostrum, 2005.

2006

49. Danny Ablahad, Development environment for single chip computers intended for simulation of CAN communication, School for Information and Communication Technology, masters thesis, Stockholm, Sweden, October 2006.
50. Solmaz Ghaznavi, Multi-IP-Based SoC Design Including CCM Security Mode of Operation, masters thesis, School for Information and Communication Technology, Stockholm, Sweden, August 2006.

51. Kashif Saeed, Design of a Power Saving Methodology for Next Generation Wireless System-on-Chip Design, masters thesis, School for Information and Communication Technology, Stockholm, Sweden, May 2006.
52. Matthias Bauhofer, Load Balancing for Power Minimization in Networks on Chips, masters thesis, School for Information and Communication Technology, Nostrum, Stockholm, Sweden, April 2006.
53. Mathias Meyer, Energy-Aware Task Allocation for Network-on-Chip Architectures, masters thesis, School for Information and Communication Technology, Nostrum, Stockholm, Sweden, March 2006.
54. Dimitris Tsaimos, UMTS Gi Interfacing and Measuring System, masters thesis, School for Information and Communication Technology, Stockholm, Sweden, January 2006.
55. Liang Zhou, Integration of ISS Simulation and NoC Simulation, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Nostrum, Stockholm, Sweden, December 2006.
56. Naresh Vendra and Karthik Chaluvadi, Decimation Filter for the VACS Platform, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, IMIT/ECS-2006-132, December 2006.
57. Anand Pendem and Rajesh Garikipati, Digital Filters for Bio-Signal Processing in the VACS Platform, masters thesis, School for Information and Communication Technology, Stockholm, Sweden, November 2006.

2007

58. Niklas Molin, Bussarkitektur i FPGA system, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2006-133, February 2007.
59. Raghavendra Ravi Chandravatti, Design and Implementation of Navigation Controller For Unmanned Micro Autonomous Aerial Vehicle, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-11, March 2007.
60. Henrik Tengstedt, High Precision Motor and Servo Controller For Unmanned Micro Autonomous Aerial Vehicle, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-19, March 2007.
61. Awet Yemane Weldezion, Vital Signs Acquisition and Communication System Board Implementation, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-142, December 2007.
62. Lin Qiu, System-level power management design on portable multimedia device, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-123, November 2007.
63. Shuo Yang, Design and Implementation of an FPGA Based Realtime Event Selector for Relativistic Heavy-ion Collision Experiments, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-106, August 2007.
64. Jaume Serra Roig, Sting Bluetooth Control vi Motorola HT820, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-100, July 2007.

65. Xu Xun, Schematic Design of an FPGA-Based Network on Board, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-91, July 2007.
66. Lu Lu, Implementation of Acoustic Echo Cancellation for PC Applications using Matlab, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-63, July 2007.
67. Li Shuo, Embedded Compression Algorithm Study for alpha RGB Graphics Content, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-54, June 2007.
68. Xue Yang, Mapping Applications onto Networks-on-Chip with a Genetic Algorithm, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-55, June 2007.
69. Pablo Fernandez Carmona, A study on transactors in multi language, mixed-level simulation of digital electronic systems, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-53, May 2007.
70. Lei Xia, Simulated Annealing Techniques for Mapping Cores onto 2-D Mesh Network on Chip, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-56, May 2007.
71. Talasila Indira Priyadarshini, Implementation of Re-configurable Analog Circuitry on Field Programmable Analog Array for Vital Signs Acquisition and Communication System (VACS) Platform, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-32, April 2007.
72. Yan Yan, Hardmotion Design, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-88, July 2007.

2008

73. Alexandre Campos, Prototyping of a Memory Subsystem on FPGA to interface to Flash Memories, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2008-131, December 2008.
74. Dimitrios Brachos, Implementation of a DLI-Guard using the AMBA AXI Protocol for Network-on-Chip, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2008-118, December 2008.
75. Xinyou Tian, Implementation of Message Scheduling on TDM Virtual Circuits for Network-on-Chip, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2008-98, November 2008.
76. Xingya Zhou and Tobias Hedlund, Correlation and Graphical Presentation of Event Data from a Real-Time System, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2008-93, November 2008.
77. Ashkan Beyranvand Nejad, High-Level Debugger Software for Communication-Centric Transaction-Based Debug Infrastructure of Systems on Chip (AEthereal

- Platform), masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2008-100, October 2008.
78. Alexander Wei Yin, Generalization of Slot Table Size for Virtual Circuits on Network-on-Chip, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2008-41, June 2008.
 79. Seyed Hosein Attarzadeh Niaki, Integrating FPCA in a Reconfigurable Logic, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2008-21, June 2008.
 80. Xiuliang Wang, Incremental embedded system development based on an RTOS, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, KTH/ICT/ECS-2008-31, June 2008.
 81. Vitaliy Kuhar, CORDIC IP Block Design, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2008-16, April 2008.
 82. Selim Erten, Development and Evaluation of a Memory Consistency and Cache Coherence Protocol for the Nocsim NoC Simulator, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2007-125, February 2008.

2009

83. Davit Mirzoyan, Fault-Tolerant Memories in FPGA based Embedded Systems, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, October 2009.
84. Jiayi Zhang, Design and Implementation of AXI-based Network-on-Chip Systems for Flow Regulation, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, TRITA-ICT-EX-2009:157, October 2009.
85. Zubair Wadood Bhatti, A Radio-Frequency and Body-Coupled Communication Dual Technology Wireless Sensor System Architecture, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, TRITA-ICT-ECS-2009:112, September 2009.
86. Aida Naluwoza, Investigation of A/D Converters for Implantable Devices, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, TRITA-ICT-ECS-2009:7, June 2009.
87. Naveed Ahmed, An Authentication Framework for Nomadic Users in Ubiquitous Computing, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, TRITA-ICT-ECS-2009:11, May 2009.
88. Chen Jing, Integration of Mathworks Simulink in a Tool for Model Based Development, masters thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, ICT/ECS-2008-076, February 2009.

6.5 Ph.D. Thesis supervision

- Mattias O'Nils, *Specification, Synthesis and Validation of Hardware/Software Interfaces*, Ph.D. thesis, Royal Institute of Technology, Sweden, June 1999.

- Per Bjureus, *High-Level Modeling and Evaluation of Embedded Real-Time Systems*, PhD thesis, Department of Microelectronics and Information Technology, Royal Institute of Technology, Stockholm, Sweden, TRITA-IMIT-LECS-02-03, June 2002.
- Ingo Sander, *System Modeling and Design Refinement in ForSyDe*, PhD thesis, Department of Microelectronics and Information Technology, Royal Institute of Technology, Stockholm, Sweden, TRITA-IMIT-LECS AVH 03:03, May 2003.
- Abhijit Kumar Deb, *System Design for DSP Applications with the MASIC Methodology*, PhD thesis, Royal Institute of Technology, Stockholm, September 2004. (Cosupervision)
- Tarvo Raudvere, *Verification of Local Design Refinements in a System Design Methodology*, Licentiate thesis, Royal Institute of Technology, Stockholm, April 2004.
- Zhonghai Lu, *Using Wormhole Switching for Networks on Chip: Feasibility Analysis and Microarchitecture Adaptation*, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, Licentiate thesis, June 2005.
- Zhonghai Lu, *Design and Analysis of On-Chip Communication for Network-on-Chip Platforms*, PhD thesis, Royal Institute of Technology, Stockholm, ISBN 978-91-7178-580-0, TRITA-ICT/ECS AVH 07:02, March 2007.
- Tarvo Raudvere, *System Level Techniques for Verification and Synchronization after Local Design Refinements*, PhD thesis, Royal Institute of Technology, Stockholm, ISBN 978-91-7178-677-7, TRITA-ICT/ECS AVH 07:05, August 2007.
- Iyad Al-Khatib, *Performance Analysis of Application-Specific Multicore Systems on Chip*, PhD thesis, Royal Institute of Technology, Stockholm, ISBN 978-91-7178-960-0, TRITA-ICT/ECS AVH 08:06, June 2008.
- Jun Zhu, *Energy and Design Cost Efficiency for Streaming Applications on Systems-on-Chip*, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, Licentiate thesis, May 2009.
- Huimin She, *Network-Calculus-based Performance Analysis for Wireless Sensor Networks*, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, Licentiate thesis, June 2009.
- Ming Liu, *A High-end Reconfigurable Computation Platform for Particle Physics Experiments*, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, Licentiate thesis, November 2008.

6.6 Thesis evaluation, opponent

- I was opponent to the following Licentiate defences:
 - Erik Stoy, *A Petri Net Based Unified Representation for Hardware/Software Co-Design*, Licentiate thesis, Linköping University, 1995.
 - Tomas Henriksson, *Hardware Architecture for Protocol Processing*, Institute of Technology, Linköping University, Linköping, Sweden, Licentiate thesis, December 2002.
 - Luis Alejandro Cortes, *A Petri Net based Modeling and Verification Techniques for Real-Time Embedded Systems*, Institute of Technology, Linköping University, Linköping, Sweden, Licentiate thesis, December 2002.
 - Filip Sebek, *Instruction Cache Memory Issues in real-time Systems*, Department of Computer Science and Engineering, Mälardalen University, Västerås, Sweden, Licentiate thesis, September 2002.

- Per Andersson, *Modelling and Implementation of a Vision System for Embedded Systems*, Licentiate thesis, Department of Computer Science, Lund University, Lund, Sweden, LU-CS-LIC:2003-1, January 2003.
- Benny Thörnberg, *Memory Modeling and Synthesis for Real-time Video Processing Systems*, Mid Sweden University, 2004.
- I was opponent and expert evaluator for the following Ph.D. Theses:
 - Juha Plosila, *Self-Timed Circuit Design - The Action System Approach*, University of Turku, Turku, Finland, June 1999.
 - Tiberiu Seceleanu, *Systematic Design of Synchronous Digital Circuits*, PhD thesis, Turku Centre for Computer Science, Turku, Finland, TUCS Dissertations No 32, May 2001.
 - Dag Björklund, *A Kernel Language for Unified Code Synthesis*, Turku Center for Computer Science, February 2005.
 - Basant Kumar Dwivedi, *Synthesizing Application Specific Multiprocessors Architectures for Process Networks*, IIT Delhi, New Delhi, India, 2005.
 - David Sigüenza Tortosa, *Proteo: The Development of a Practical Network-on-Chip*, Tampere University of Technology, Tampere, Turku, 2005.
 - Heikki Kariniemi, *ON-LINE RECONFIGURABLE EXTENDED GENERALIZED FAT TREE NETWORK-ON-CHIP FOR MULTIPROCESSOR SYSTEM-ON-CHIP CIRCUITS*, Tampere University of Technology, Tampere, Finland 2006.
 - Xin Wang, *Designing Globally-Asynchronous Locally-Synchronous On-Chip Communication Networks*, Tampere University of Technology, Tampere Finland 2008.
- I have served on the evaluation committees for the following Ph.D. defenses:
 - Ingemar Söderquist, *CMOS Circuits for Digital Systems*, PhD thesis, Department of Electrical Engineering, Linköping University, Dissertation No. 775, October 2002.
 - Paul Popp, *Analysis and Synthesis of Communication Intensive Heterogeneous Real-Time Systems*, PhD thesis, Institute of Technology, Linköping University, Dissertation No. 833, June 2003.
 - Daniel Eckbert, *Power Estimation and Multi-Phase Clock Generation for the Deep Submicron Era*, Department of Computer Engineering School of Computer Science and Engineering, Chalmers University of Technology, Göteborg, Sweden, December 2003
 - Joe Armstrong, *Making reliable distributed systems in the presence of software errors*, PhD thesis, Department of Microelectronics and Information Technology, Royal Institute of Technology, November 2003.
 - Ulf Nordqvist, *Protocol Processing in Network Terminals*, Linköping University, 2004.
 - Luis Cortes, *Verification and Scheduling Techniques for Real-time Embedded Systems*, Linköping University, Sweden, 2005.
 - Paul Pop, *Analysis and Synthesis of Communication-Intensive Heterogeneous Real-Time Systems*, Ph. D. Thesis No. 833, Dept. of Computer and Information Science, Linköping University, June 2003
 - Sorin Manolache, *Analysis and Optimisation of Real-Time Systems with Stochastic Behaviour*, Linköping University, Linköping, Sweden 2005.
 - Benny Thörnberg, *Memory Modeling and Synthesis for Real-Time Video Processing Systems*, Mid-Sweden University, Sundsvall, Sweden 2006.
 - Antonis Papanikolaou, *Application-driven Software Configuration of Communication Networks and Memory Organizations*, Gent University, Belgium 2006.
 - Sander Stuijk, *Predictable Mapping of Streaming Applications on Multiprocessors*, Technical University Eindhoven, The Netherlands, November 2007.

- Martin Holzer, *Design Space Exploration for the Development of Embedded Systems*, Vienna University of Technology, Vienna, Austria 2008.
- Ari Kulmala, Scalable Multiprocessor System-on-Chip Architecture Design on FPGA, PhD thesis, Tampere University of Technology, Tampere, Finland, 2008.
- Najeem Lawal, Memory Synthesis for FPGA Implementation of Real-Time Video Processing Systems, PhD thesis, Mid Sweden University, Sundsvall, Sweden, ISBN 978-91-86073-26-8, January 2009.
- Wang Xin, Designing Globally-Asynchronous Locally-Synchronous On-Chip Communication Networks, PhD thesis, Tampere University of Technology, Tampere, Finland, 2008.
- Fernando Herrera Casanueva, Heterogeneous Specification and Automatic Software Generation from SystemC for Embedded Systems, PhD thesis, University of Cantabria, Santander, Spain, January 2009.

6.7 Publications on education

I have co-authored several papers and made a few presentations relating to education. The papers are in the publication list, but I also include them in the following summary.

- L. Hellberg, A. Hemani, J. Isoaho, A. Jantsch, M. Mokhtari, and H. Tenhunen, "System Oriented VLSI Curriculum at KTH", *Proceedings of the International Conference on Microelectronic Systems Education, MSE97*, 1997.
- L. Hellberg, A. Hemani, J. Isoaho, A. Jantsch, M. Mokhtari, and H. Tenhunen, "Integration of Physical and Functional Electronic System Representations in Electronic Curriculum", *Proceedings of the 15th NORCHIP Conference*, 1997.
- *System-on-chip education*. Panel Presentation at NorChip 2000, Turku, Finland, November 2000.
- *International master of science program in system-on-chip design at KTH*. Presentation at System-on-Chip Design at the Graz University of Technology, Graz, Austria, April 2001.
- *Industrial Ph.D. projects*. Presentation at the Industrial Research Seminar at SaabTech, Stockholm, Sweden, September 2001.
- *Embedded software/system in the SOC Master program*. Presentation at the Socware Education workshop, November 2001.
- Tero Nurmi, Hannu Tenhunen, Li-Rong Zheng, Axel Jantsch, Jari Nurmi, and Jouni Isoaho, "Physical Performance Modelling for Platform-based SoC Design", 4th European Workshop on Microelectronics Education, May 2002.
- Ingo Sander, Axel Jantsch, and Hannu Tenhunen, "The Platform as Interface in a SoC Design Curriculum", *Proceedings of the 5th European Worksop on Microelectronics Education*, Lausanne, April 2004.
- Axel Jantsch, Exchange of Course Modules across Universities, Invited presentation at the 6th European Workshop on Microelectronic Education, June 2006.

6.8 Other Activities in Education

- In autumn 1998 I was consultant in the definition process for the fourth year of the master program *Embedded Systems* at the Jönköping Ingenjörshögskolan. In 1999 a master of science education in *Embedded Systems* has been established for the first time at the Ingenjörshögskolan in Jönköping. Therefore, a fourth year had to be defined on top of the three year education programs already in place. I was thoroughly involved

in this process and much of the current curriculum structure and many courses are based on my proposal.

- In 2000 I contributed to the definition of the Royal Institute of Technology's IT-University curriculum in the circuits and systems line.
- In 2000 I contributed to the definition of the Royal Institute of Technology's Master Program in System-on-Chip, which has been further developed since then with my active participation and contribution.
- Since October 2006 I am responsible director for the International Master Program "System on Chip Design".

7. Other Professional Activities

7.1 PC member

- DATE (Design Automation and Test in Europe) 2001-2005, 2008, 2009
- FDL (Forum on Design Languages) 1998 -2003
- HDLCON (Hardware Description Language Conference) 2000
- DCC (Designing Correct Circuits) Workshop 2004
- CODES-ISSS 2003-2008, PC Co-chair in 2004, general co-chair 2005, member of the steering committee since 2006.
- SoC Symposium 2003-2008
- TPC Co-chair for the DATE Workshop on "Diagnostic Services in Network-on-Chips". April 2007.
- TPC Co-chair for the DAC Workshop on "Diagnostic Services in Network-on-Chips". June 2008.
- Member in steering and program committee of the International Symposium on Networks on Chip, 2007, 2008, 2009.
- TPC co-chair of the International Symposium on Networks on Chip, San Diego 2009.

7.2 Reviewing of journal articles:

- IEEE Transactions of VLSI, 1999-2008
- IEEE Transactions of Circuits and Systems, October 1999
- Journal of Systems Architecture, June 2000
- IEEE Transactions on CAD, 2000-2008
- Kluwer Design Automation of Embedded Systems, 2000-2002
- IEEE D&T Magazine, 2000-2008
- IEEE Computer 2002-2003
- ACM Transactions on Embedded Computing Systems, 2002, 2006-2008
- IEEE Transactions on Parallel and Distributed Systems, 2004
- IEEE Transactions on Computers, 2006, 2007
- Subject Area Editor of HW/SW Codesign for the Journal of Systems Architecture since 2002-2008
- Guest editor for the special issue on Networks on Chip in the Journal of System Architecture 2003

- Guest editor for the special section on Hardware/Software Codesign and System Synthesis in IEEE Transactions on VLSI Systems, Part I in August 2006 and Part II in September 2006.
- Guest editor for the special issue on *C based System Level Design* of the EURASIP Journal of Embedded Systems, 2008.
- Guest editor for the special issue on Networks on Chip in IEEE TCAD 2010.

7.3 Organizing of conferences and workshops

- Chairman of the Program Committee of the International Workshop on System Level Design Languages, Tübingen, Germany 2000.
- INTELECT Workshop, Linköping, Sweden, June 1999.
- INTELECT Summer Schools, ...rebro, Sweden, 2000, 2001, 2002.
- EuroTraining Course on System on Chip, 3 days, Stockholm, May 2001.
- Eda Träff, Stockholm, Sweden, 2000.
- SSoCC 2001, 2002.
- CODES-ISSS 2004 in Stockholm.
- CODES+ISSS 2005 as general co-chair in New York.
- Full day tutorial on Networks on Chip at DATE 2007.
- Full day Workshop on Diagnostic Services in Network-on-Chips at DATE 2007.
- Full day Workshop on Diagnostic Services in Network-on-Chips at DAC 2008.

7.4 Project reviews

- Dutch technology Foundation STW, 2003, 2004.
- Academi of Finland, 2004
- Engineering and Physical Science research Council, UK, 2004
- King Fahd University of Petroleum and Minerals research council, 2005.
- Vetenskapsråd, 2006 – NT-S committee.
- Vetenskapsråd, 2008 project review.
- EU FP7 Reviewer 2009, 2010
- EU Artemis reviewer 2010.

7.5 Awards

- Best paper nomination at the Forum on Design Languages, 1999.
- Best paper award at the 10th International Conference on Field Programmable Logic and Applications, August 2000.
- Best paper nomination at the Design Automation and Test in Europe Conference 2003.
- Best paper nomination at the Design Automation and Test in Europe Conference 2004.
- Best paper nomination at the Design Automation Conference (DAC) 2006.

7.6 Invited talks and seminars

1997-1999

1. "Limitations of Interactive Design", Invited presentation at *Workshop on Electronic Design Processes*, Monterey, CA, 1997.
2. "Formal System Specification and Refinement" at the FMV Workshop on Formal Methods in Electronics Design, Lida, Sweden, September 1998.
3. "System Design", EDA Gruppen regular meeting, Stockholm, December 1998.
4. "The Rugby Model" at the Indian Institute of Technology, Delhi, India, January 1999.
5. "Formal System Specification Models for Verification and Refinement", EDA-Träff'99, Stockholm, Sweden, March 1999.
6. "Integrated Electronic Systems Program - A National Research Program", EDA-Träff'99, Stockholm, Sweden, March 1999.
7. "Models of Computation and Heterogeneous Simulation" at TIMA Laboratory, Grenoble, France, September 1999.
8. "The Rugby Model: A Frame work for the study of Modelling, Analysis and Synthesis Concepts of Electronic Systems", TU Darmstadt, November 1999.
9. "Models of Computation", EDA Gruppen regular meeting, Linköping, December 1999.

2000

10. "Integrated Electronic Systems Program", EDA-Träff 2000, Stockholm, Sweden, March 2000.
11. Panel member on "Challenges in SoC Education" at the IEEE NorChip Conference, Turku, Finland, November 2000.
12. "The Integrated Electronics Systems Research Program", SSF Program Conference, Stockholm, November 2000.

2001

13. Axel Jantsch, System Modelling - Models of Computation and their Applications, Presentation at System-on-Chip Design at the Graz University of Technology (50 min), April 2001.
14. Axel Jantsch, International Master of Science Program in System-on-Chip Design at KTH, Presentation at System-on-Chip Design at the Graz University of Technology (10 min), April 2001.
15. Axel Jantsch, The Usage of Stochastic Processes in Embedded System Specifications, Presentation at the HW/SW Codesign Symposium in Copenhagen (20 min), April 2001.
16. Axel Jantsch, System Modelling - Models of Concurrency and their Applications (4h), Presentation at Jönköping University, April 2001.

17. Axel Jantsch, Introduction to Haskell and ForSyDe, Presentation at KTH (1h), March 2001.
18. Axel Jantsch, HW/SW Codesign (4h), Presentation at Jönköping University, May 2001.
19. Axel Jantsch, System Modelling and SDL-Matlab Cosimulation (2h), Presentation at the Eurotraining System-on-Chip Course, May 2001.
20. Axel Jantsch, Industrial Ph.D. Projects (30min), Presentation at the Industrial Research Seminar at SaabTech, Stockholm, Sweden, September 2001.
21. Axel Jantsch, Introduction to Networks on Chip (30min), Workshop at the European Solid-State Circuit Conference (ESSCIRC), Villach, Austria, September 2001.
22. Axel Jantsch, Network-on-Chip Architectures (30min), Workshop at the European Solid-State Circuit Conference (ESSCIRC), Villach, Austria, September 2001.
23. Axel Jantsch, Models of Computation in Embedded System Design (50 min), Presentation at the Department of Computer Science at Linköping University, September 2001.
24. Axel Jantsch, Embedded Software/System in the SOC Master Program, Presentation at the Socware Education workshop, November 2001.

2002

25. Axel Jantsch, A Template for Distance Learning Courses without Loss of Quality, Presentation at the SoC SME Workshop, April 2002.
26. Axel Jantsch, Networks on Chip, Presentation at the Conference RadioVetenskap och Kommunikation, June 2002.
27. Axel Jantsch, Networks on Chip: A Paradigm Change?, Presentation at the SOCWare Day, Kista, November 2002.
28. Axel Jantsch, Network on Chip Architecture, Presentation at the EXCITE Workshop, Helsinki, November 2002.
29. Axel Jantsch, Networks on Chip, Presentation at the SoC Architecture Course at KTH, December 2002.

2003

30. *Networks on chip - status of Nostrum*. Invited Presentation at Darmstadt University of Technology, April 2003.
31. *What is a good platform?* Presentation at the EDA Gruppen Meeting, February 2003.
32. *Communication Refinement for a Network-on-Chip Platform*, Invited presentation at MPSOC'03 - International Seminar on Application- Specific Multi-Processor SoC, Chamonix, France, July 2003.
33. *Networks on Chip*, Invited keynote at DSD'2003 - Euromicro Symposium on Digital System Design, September 2003.
34. *System Specification Fundamentals*, Invited presentation at the Medea+ DAC Conference, Stuttgart, November 2003.

35. *Network on Chip Tutorial*. Invited lecture at the Stringent Summer School, August 2003, Örebro, Sweden.
36. *Networks on Chip*. Invited tutorial at the IEEE NorCHIP Conference, Riga, Latvia, November 2003.
37. *The Nostrum network on chip*. Invited presentation at ProRISC, Eindhoven, November 2003.

2004

38. The Nostrum network on chip. Guest lecture in the SoC Architecture course, KTH, December 2004.
39. Networks on chip. Invited seminar at Linköping University, November 2004.

2005

40. The Nostrum network on chip. Invited Seminar at Åbo Akademi, Turku, Finland, March 2005.
41. Axel Jantsch, Robert Lauter, and Arseni Vitkowski. *Power analysis of link level and end-to-end protection in networks on chip*. Invited presentation for the special session on Networks on Chip at ISCAS, May 2005.
42. The Nostrum network on chip. Invited presentation at the International Symposium on System-on-Chip, Tampere, Finland, November 2005.
43. The Nostrum network on chip. Invited presentation at Lancaster University, October 2005.
44. NoC: A new contract between hardware and software? Invited seminar at Lancaster University, October 2005.

2006

45. Compositional traffic in networks on chip. Invited presentation at the Baltic Electronic Conference, October 2006.
46. Communication performance in network-on-chips. Short course at Tallinn Technical University, October 2006.
47. Exchange of course modules across universities. Invited presentation at the 6th European Workshop on Microelectronic Education, June 2006.
48. Models of computation for networks on chip. Invited talk at the Sixth International Conference on Application of Concurrency to System Design, June 2006.
49. Standards for NoC: What can we gain? Invited presentation at the DATE Workshop on Future Interconnect and NoC, March 2006.
50. Tiberius Seceleanu, Axel Jantsch, and Hannu Tenhunen. On-chip distributed architectures. Tutorial at the International SoC Conference, September 2006. Austin, Texas.
51. Axel Jantsch, ForSyDe: A Denotational Framework for Heterogeneous Models of Computation, Invited Presentation at the ARTIST workshop Models of Computation and Communication, November 2006.

2007

52. Axel Jantsch, NoC: State of the art, trends and challenges, Section I of Full Day Tutorial "NoC at the Age of Six: Advanced Topics, Current Challenges and Trends" at DATE 2007, April 2007.
53. Axel Jantsch, Performance analysis and dimensioning of bandwidth and buffer capacity, Section I of a full day tutorial "Tutorial on Networks on Chip" at the NoC Symposium 2007, May 2007.
- [1] Axel Jantsch, Models of Computation for Networks on Chip, Invited Seminar at IMEC, February 2007.
- [2] Axel Jantsch and Zhonghai Lu, Slot allocation using logical networks for TDM virtual circuit configuration for network-on-chip, Invited Seminar at Eindhoven University of Technology, November 2007.
- [3] Axel Jantsch, The Nostrum Network on Chip, Invited Seminar at Turku Center for Computer Science, November 2007.
54. Axel Jantsch, *Network Layer Communication Performance in Network-on-Chips*, Section I of a half day tutorial "Tutorial on Networks on Chip" at the ASP-DAC 2008, January 2007.

2008

- [4] Axel Jantsch, Network Layer Communication Performance in Networks on Chip, Tutorial at the Asian Pacific Design Automation Conference, January 2008.
55. Axel Jantsch, *A Formal Framework for Heterogeneous Models of Computation*, Section I of a half day tutorial at DATE, March 2008.
- [5] Axel Jantsch, Nostrum Network on Chip, Invited Seminar at the Turku center of Computer Science, April 2008.
- [6] Axel Jantsch and Zhonghai Lu, Quality of Service in Networks on Chip, Invited Seminar at the Research Center Telecommunication Vienna (FTW), April 2008.
- [7] Axel Jantsch. Nostrum network on chip. Invited Seminar at the Turku center of Computer Science, April 2008.
- [8] 2009
- [9] Axel Jantsch and Zhonghai Lu. Trends in terascale on-chip computing 2010-2020. Invited Seminar at the ICES annual conference, September 2009.
- [10] Axel Jantsch and Zhonghai Lu. Trends in terascale on-chip computing 2010-2020. Invited Seminar at Nanjing University, July 2009.
- [11] Axel Jantsch et al. The Nostrum network on chip. Invited Seminar at Fudan University, June 2009.
- [12] Axel Jantsch and Zhonghai Lu. Networks on chip. Short course at Fudan University, June 2009.
- [13] Axel Jantsch. Resource allocation for quality of service on-chip communication. Invited seminar at the University of Cantabria, Santander, Spain, February 2009.
- [14] Axel Jantsch. Resource allocation for quality of service on-chip communication. Invited seminar at the real Time Research Center in Vasteras, Sweden, February 2009.

8. Contributions in Research:

First, I list results from my research activities, then I provide a summary and my assessment of this work.

- Development of a lexicon organization and an analysis algorithm for German syntax as part of my Master thesis.
- Development of a family of estimation functions for area and performance of hardware circuits from a behavioural descriptions as part of my PhD thesis.
- Development of formal notation to describe design decisions in the hardware design process, called a design style description language, as part of my PhD thesis.
- Development of a HW/SW codesign system, named Akka, as a post doctoral scholar at KTH, 1993-1995. The main contributions were a partitioning algorithm based on dynamic programming, a cosimulation environment, a coemulation environment, a profiling method for performance estimation, and a graphical front-end to visualize design properties. This activity eventually led to 1 Licentiate thesis, 1 PhD thesis, a few Master theses, and essentially initiated the HW/SW codesign activity at the Royal Institute of Technology.
- Development of a system level testcase specification and development method and a formal testcase partitioning technique together with Thomas Albrecht and Johan Notbauer at Siemens Austria AG in 1996-1998.
- Development of a HW/SW interface synthesis and validation method together with the Ph.D. student Mattias O’Nils at the Royal Institute of Technology 1997-1999.
- Co-development of an internal representation for system design (IRSYD) at the Royal Institute of Technology in 1997-1999.
- Development of a general conceptual frame (the *Rugby Model*) to study problems in the modelling and design of electronic systems together with Shashi Kumar and Ahmed Hemani at the Royal Institute of Technology 1997-1998.
- Development of the theoretical foundation and a practical implementation of an SDL-Matlab comodelling, cosimulation and performance estimation system (MASCOT) together with Ph.D. student Per Bjureus at the Royal Institute of Technology in 1998-2002.
- Development of the concept and architecture of a General Purpose Protocol Processor together with Ahmed Hemani, Johnny Öberg and Yutai Ma, 1998-2002.
- Co-development of the MASIC (Math to ASIC) methodology, that systematically separates global control, timing and configuration issues from the datapath, together with Abhijit Kumar Deb and Ahmed Hemani. 2001-2003.
- Development of a formal framework for models of computation that is based on deterministic process networks. Based on the concepts described in *Modeling Embedded Systems and SoCs - Concurrency and Time in Models of Computation*, Morgan Kaufmann Publishers, June 2003, the ForSyDe modelling and design methodology has been developed together with Ph.D. students Ingo Sander, Wenbiao Wu, Tarvo Raudvere, Ashish Singh, Zhonghai Lu and Jun Zhu at the Royal Institute of Technology, 1997-ongoing.
- Development of Nostrum, the KTH Network on Chip together with Ahmed Hemani, Shashi Kumar, Zhonghai Lu, Mikael Millberg, Erland Nilsson, Richard Thid, Johnny Öberg and others. Nostrum is based on a buffer-less, loss-less minimal switch architecture that offers both best effort and guaranteed bandwidth services. 2000-ongoing.

Since my doctoral thesis in 1992 I have been working on various problems in the area of design of hardware and mixed hardware/software systems. Embedded systems and

systems on a single chip belong to this class of systems. My focus has been on the system level, rather than the implementation or technology level, of such systems. The work has addressed problems in synthesis, estimation, simulation, modelling, validation, and specification.

An important component in my work is the aspiration to thoroughly understand the fundamental aspects of design problems and to put design methods on a formal, if possible mathematical, foundation. This aspiration however, goes together with the ambition to develop techniques that can address and solve design problems within 2-5 years and that can be used by engineers in practise. An example where this dual ambition could be successfully met, is MASCOT. MASCOT connects Matlab and SDL descriptions in an integrating modelling and simulation framework. Matlab and SDL are very different design languages, used by different communities for different tasks and different parts of a system. However, these different parts have to be evaluated and validated together. MASCOT is based on a formally defined communication and synchronization mechanism, called the composite signal flow, and is a practical tool which allows an engineer to integrate Matlab and SDL descriptions in a transparent way. The tool is now being evaluated in design projects at Saab Dynamics.

However, MASCOT and other similar, more or less successful examples of individual techniques and tools, can only solve isolated problems, although in a clean and sophisticated way. More fundamentally, the design process has to be viewed as an integrated whole, the foundation of which are the modelling concepts and languages. The selection of modelling concepts, semantics and languages fundamentally determine the potential and limitations of synthesis, verification, and estimation techniques. Due to the wide variety of design tasks with very different requirements on the modelling concepts the selection or design of a modelling language, suitable and efficient for all important design tasks, is hard. Examples of achievements towards this long term goal are the development of the Rugby meta model, the ForSyDe methodology and an integrating framework for models of computation described in my recent book.

The Rugby meta-model is the result of a thorough analysis of design domains and abstraction levels. Rugby separates every design description into the four domains computation, communication, data and time. In each domain exist several abstraction levels ranging from system level constraints to technology related implementation concepts. It turns out that all design activities can be concisely described with Rugby concepts. For instance synthesis activities are refinements from one abstraction level to another in one or several domains. Thus, Rugby is a useful meta-model to describe and comprehend design activities and methodologies.

ForSyDe (stands for Formal System Design) is a formally defined system specification method and a refinement methodology. Its salient features are the conceptually strict separation of computation, communication and data, which can be optimised and refined separately, and the systematic refinement along the time domain towards increasingly lower time abstractions and higher time accuracy. ForSyDe is a long term endeavour and by far not yet completed but a few interesting results have already been accomplished. Internationally recognized achievements include a formal communication and interface refinement method and a systematic treatment of purpose, usage and interpretation of nondeterminacy, stochastic and deterministic behaviour in system design. In May 2003 Ingo Sander has defended his Ph.D. thesis on this topic.

Nostrum is a Network-on-Chip (NoC) architecture developed at KTH. During the last 5 years we have developed the basic architecture, topology, a switch and routing policy, a protocol stack from the data link to the session layer, and a communication refinement

method. Most of our solutions are still incomplete and will be developed further, but we have laid the foundation of a complete NoC platform that is an excellent frame for our research on various point problems. Nostrum has obtained significant international attention which has resulted in a number of invited presentations.

9. Experience in Organization and Management:

- I conducted and led several 0.5 to 2 man-year projects to develop module generators and one ASIC between 1988 and 1992.
- Leader of the project *Performance Estimation* in 1993-1995 under the umbrella of the *Advanced ASIC Consortium*, a research organization jointly run by industry and University representatives with the objective to develop methods and tools for design of telecom systems.
- Representative of Siemens Austria in the FOST project, an EU financed research project, in 1996.
- Leader of the project HW/SW Codesign since January 1997 under the umbrella of the *Advanced ASIC Consortium II*, a research organization jointly run by industry and University representatives with the objective to develop methods and tools for design of telecom systems.
- Project leader of a research project in collaboration with Celsius Tech Electronics on System Specification and Property Estimation since January 1998.
- KTH representative in the *Advanced ASIC Consortium II* since August 1998.
- Deputy Head of Laboratory (Biträdande avdelningschef) at the Electronics System Design Laboratory (ESDlab), Department for Electronics (ELE), KTH, May - December 1998.
- January 1999-December 2002 I was general manager of SSF's (Stiftelsen för strategisk forskning) program *Integrated Electronic Systems*, which involves groups from four Universities (KTH, LiTH, LTH, CTH) and has a four year budget of 110 MSEK.
- Since June 2002 I have been leader of the SAM (System Architecture and Methodology) Group at KTH. This position includes technical, personal and financial responsibilities. As of today the group consists of three senior researchers and ten Ph.D. students.
- January 2004-September 2005 I was head the Laboratory for Electronics and Computer Systems (LECS), which hosted 8 professors and in total 65 persons. As head I had financial and personell responsibility.
- Since July 2009 I am head of Electronic Systems Department with 60 persons.

10. Grants and research contracts

Research grants:

Project name	Period	Funding Agency	Amount	Note
Schrödinger Scholarship	1993-1995	Austrian Science Foundation	600 k...S	
AASIC Consortium	1997-1999	SSF (Strategic Research Foundation)	2500 kSEK	Industrial participation

SAVE	1998-2000	NUTEK	1333 kSEK	50% industrial cofinancing
Protocol Processor	1999-2002	SSF/Intelect	2400 kSEK	Industrial participation
MASIC	1999-2002	SSF/Intelect	1800 kSEK	Industrial participation
Low Power Operating Systems	2000-2003	SSF/Intelect	1800 kSEK	Industrial participation
System Specification and Verification	2001-2003	SSF/Intelect	1200 kSEK	Industrial participation
Formal System Design	1999-2003	SSF/Intelect	1600 kSEK	Industrial participation
NOCARC	2001-2003	Vinnova	3000 kSEK	50% industrial cofinancing
NOC Design Methodology	2001-2004	SOCWare	2250 kSEK	Industrial participation
NOC Evaluation	2002-2005	SOCWare	1500 kSEK	Industrial participation
SOC-SME	2002-2004	Nordisk Industri Fond	900 kNOK	50% cofinancing
SOC-Mobinet	2002-2004	EU	870 kEuro	50% industrial cofinancing; Main applicant: H. Tenhunen
SPRINT	2006-2008	EU	304 kEuro	IP project, Philips Semiconductor is coordinator
ANDRES	2006-2008	EU	223 kEuro	STREP project, OFFIS is coordinator
HET-MoC	2006-2008	Swedish Research Council	2200 kSEK	
MOSART	2008-2011	EU	247 kEuro	STREP project, Thales is coordinator
SYSMODEL	2009-2011	EU Artemis	360 kEuro	Artemis project

NoC ADM	2009-2011	Swedish Resarch Council	2400 kSEK	
iFEST	2010-2012	EU Artemis	300 kEuro	Artemis project, ABB is coordinator

Research contracts:

- MASCOT, SaabTech, 1998-2002, 600 kSEK + fulltime Ph.D. student
- ArchDes, Jönköping School of Engineering, 1999-2000, 400 kSEK + fulltime Ph.D. student
- SaverNOC, SaabTech, 2005-2007, 360 kSEK + fulltime Ph.D. student

11. Reviewed International Publications

Many of the following publications have been written in cooperation with others. If I am the first author, the initiative, problem definition and major part of the solution have been accomplished by me. In joint papers with my graduate students I have supervised their work, I have jointly with them decided the research direction and formulated the problem, and I have contributed to the solution in regular discussions. In all other papers, my contribution was sometimes minor, sometimes significant, but I have typically not initiated the work.

1992-1993

- [15] Axel Jantsch, Design Space Exploration with Design Style Description and Estimation Functions, Ph.D. thesis, Technische Universität Wien, Institut für Technische Informatik, September 1992.
- [16] Axel Jantsch, "Capability Library for High Level Synthesis", Proceedings of the Workshop on Control Dominated Synthesis, Dresden 1992.
- [17] Axel Jantsch, "Hades: An Environment for Design Space Exploration", Proceedings of GME Fachtagung *Mikroelektronik*, March 1993.

1994

- [18] Axel Jantsch, Peeter Ellervee, Johnny ...berg, Ahmed Hemani, and Hannu Tenhunen, "Software Oriented Approach to Hardware/Software Codesign", Proceedings of the Poster Session of CC'94, International Conference on Compiler Construction, Edinburgh, April 1994.
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