Rapid Energy Transfer
to an Energy Buffer

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Abstract (ENGLISH)

This master thesis introduces a new technology applicable to nearly all mobile and portable electrical devices since all of them need energy to operate. This thesis attempts to cut the last wire - this one the wire to the primary power source. In other words, fast and efficient wireless energy transference through a strong, focused near magnetic field whose fast attenuation will avoid interference with surrounding communication systems or human harm. This energy is transferred to and will be stored inside the mobile device where nothing but a small and simple secondary circuit has been placed.

The thesis project began by creating an initial SPICE computer model, providing an easy and rapid way of testing both convergence and feasibility of the topology as the design evolved from the well-known and widely used Switch Model Power Supply technology through to the detailed design and implementation of the prototype, including supporting the iterative process of testing and optimizing, all stages are carefully described in the document. The thesis shows both theoretically and practically that this idea is feasible and capable of power transmission.

Sammanfattning

Detta examensarbete introducerar en ny teknologi som är applicerbar till de flesta mobila och portabla elektriska apparater då dessa behöver energi för att fungera. Detta arbete försöker klippa den sista ledningen den som leder till den primära kraftkällan. Med andra ord, är denna teknik en snabb och effektiv trådlös energiöverföring genom ett starkt, fokuserat närbeläget magnetfält. Tack vare magnetfältets kraftiga dämpning undviks interferens med intilliggande kommunikationssystem eller personskador. Denna energi är överförd till, och lagras inuti en bärbar apparat där endast en liten och enkel sekundärkrets har placerats.

Examensarbetsprojektet påbörjades med skapandet av en inledande SPICE datormodell. Modellen möjliggjorde ett enkelt och snabbt sätt att testa både konvergens och genomförbarhet av topologin samtidigt som designen utvecklades från den välkända och vitt använda Switch Power Supply-teknologin till den detaljerade designen och implementationen av prototypen. Modellen stöttade samtidigt den iterativa processen av test och optimering. Alla faser är utförligt beskrivna i rapporten och arbetet visar både teoretiskt och praktiskt att denna idé är genomförbar och möjliggör kraftöverföring.

Table of Contents

Table of Figures

Table of Tables

List of Abbreviations and Acronyms

B	Magnetic flux density or magnetic field, measured in units of tesla (T)
CCMPWM	Current Controlled Mode Pulse Width Modulator
FB	Feedback
f_{SW}	Switching frequency
H	Magnetic field strength, measured in units of Amperes per meter (A/m)
N_P	Number of turns of wire wound around the primary core forming the primary transformer arm, generating the magnetic field
N_S	Number of turns of wire wound around the secondary core forming the secondary transformer arm, taking energy from the generated field and charging the capacitor
N_T	Number of turns of wire wound around the primary core forming the tertiary transformer arm, providing feedback about the field
P	Primary arm of the flyback transformer
RFID	Radio Frequency Identification technology
S	Secondary arm of the flyback transformer
SMPS	Switch Mode Power Supply
T	Tertiary arm of the flyback transformer
M	Magnetic permeability
Φ	Magnetic flux, measured in units of weber (Wb)

1. Introduction

Although the new functionalities of mobile information technology (IT) devices seem to be limitless, batteries are still their weak point, thus this project studies a new way to wirelessly power mobile devices. As an evolution of the RFID tags' wireless powering procedure [11] where a passive tag can transmit data back by backscattering the field provided by the reader, new questions arise:
- If a near field effect will be used for some data exchange function, how much energy can be transferred to the mobile device at the same time?
- Can enough energy be transferred to power the device for a significant amount of time?

This design moves away from existing wireless chargers adapted to battery charging requirements, and innovates, by focusing on fast energy transfer based upon an intense, focused, and rapidly attenuated magnetic field produced with high magnetic permeability, μ, materials and operated in the near field, $d<0.16\lambda$. The assumption is that energy will be buffered in a (super)capacitor ready to use. The problem this study addresses is how much useful energy can be transferred in a short amount of time.

2. Background/Related Research

Wireless is a key word today for most innovative IT products, with industry efforts oriented to providing integrated services with the highest commodities and facilities for users, without bothering the users about wires. Despite wireless communications being well established, annoying fixed wires or batteries (and battery chargers) are still required to power the devices. Consequently, major players in this field consider conveniently powering the device to be an unsolved issue, but potentially a likely profitable market, hence they have explored various solutions for wireless battery charging. Companies such as WildCharge [2] [3] have developed pads upon which devices are placed and recharged through an array of metal contacts, while SplashPower [4] [5] went further, by developping contactless systems which recharge the devices through inductive coupling. Fulton improved inductive coupling based charging system with intelligent adaptative control via their eCoupled™ system [6] [7], which utilizes feedback from individual devices in real time, modifying the charging parameters as needed. There remains a need to study the efficiency of these existing systems and to improve upon them. For example, SplashPower is using the Synopsys Saber Simulator to do this [8].

As services become more performance demanding, batteries become more of a limitation: On one hand, the efficiency of the widely used Li-Ion batteries decreases as the load decreases, something that happens as a result of the miniaturization of electronics [9]. On the other hand, these batteries have very strict guidelines that establish how they must be charged [10]. Thus, instead of providing energy to something which takes so a long time to charge and has very circumscribed requirements on voltage/current levels, an alternative is to buffering

energy for future use. The basic idea is derived from a study of RFID, Radio Frequency Identification, implementations but utilizing much higher strength fields in order to provide more than just the few milliseconds of operating time which an RFID chip requires.

RFID tags are generally passive devices powered by rectification of the magnetic (H) field which transmits information back to the reader by exploiting the power of the received field [11]. Note that even in case of active tags, the batteries are only used to power the chip, while the transmission power of the transponder comes from the received field. Unlike the previously mentioned battery charging systems, RFID generally works with only low power levels [12]. While the energy is adequate for tags it is insufficient to power more general IT devices, thus the concept has to be adapted to this different purpose. The search for high power transmission through a near inductive field implemented by an existing architecture led to the examination of Switching Mode Power Supplies [13]. Some basic concepts of these power supplies will be explained next, in order to justify this choice as our starting framework.

In Switching Power Conversion, energy is **continuously drawn** from an "input source", **chopped** into packets by means of a switch (transistor), then **averaged with** the help of an **LC** circuit in order to result in a continuous (constant average) transfer of energy. The result is that a **smooth** and steady flow of energy appears at the output.
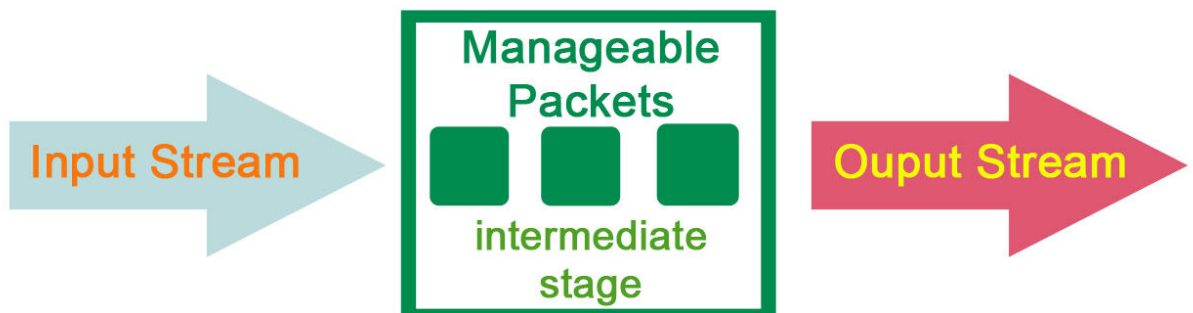
Figure 1: Switching Power Conversion

Switching Mode Power Supplies (SMPS) convert input power, provided by a DC source, into a regulated DC voltage at the output. **DC-DC SMPS** are distinguished by being highly efficient when dealing with high power conversion. This is because energy is **only consumed when switching** between the ON and OFF states**.** Energy is not consumed by the power supply itself during the ON or OFF state because the transistor has *ideally* null current flowing through it when it is OFF and because the voltage drop between its terminals is *ideally* null when it is ON. Nevertheless, real implementations always have losses due to *leakage currents*, because there's still current flowing even in the OFF state, and *conduction loss* since the voltage difference between the terminals is not null when ON. Because of their long lifetime and high switching speed, N-channel MOSFET transistors are commonly used to build these power supplies. Such a transistor is a are voltage controlled device which generates unwanted noise and ripple that require high current levels (~1A) to achieve quick

switching. As a result, a high source voltage is needed to make the device work. In addition, these devices are a source of Electro Magnetic Interference (EMI).

After reviewing all available topologies, the "*Flyback Converter*" (or "*Flyback Transformer*") [14] was chosen. Here the coil that is present in all SMPS architectures is substituted by a transformer. This seems the most suitable solution for this application because it provides electrical isolation between the primary and the secondary sides of the circuit and makes it possible to *split* **the circuit and** *separate* **both parts** so the **primary** side, containing the **controller** and all the circuitry related with the power supply can be located **at the fixed part of the circuit,** while the **secondary** (consisting of a coil, a rectifying diode, and the capacitor functioning as a buffer) will fit **inside the tiny handheld device which wishes to receive the energy**.

As a result, the innovation introduced by this research is the rapid energy transfer from a fixed device to a device which will be moving through the near inductive field existing between the primary and the secondary sides of a transformer. The final goal of this study is to predict how much energy could be coupled during a common situation, such as moving the device along an array of *primary sides* placed, for instance, in the turnstile at the entrance to the subway. As starting point, this thesis will focus on how much can be coupled from a single primary, to have an initial hint of the feasibility and performance of the system.
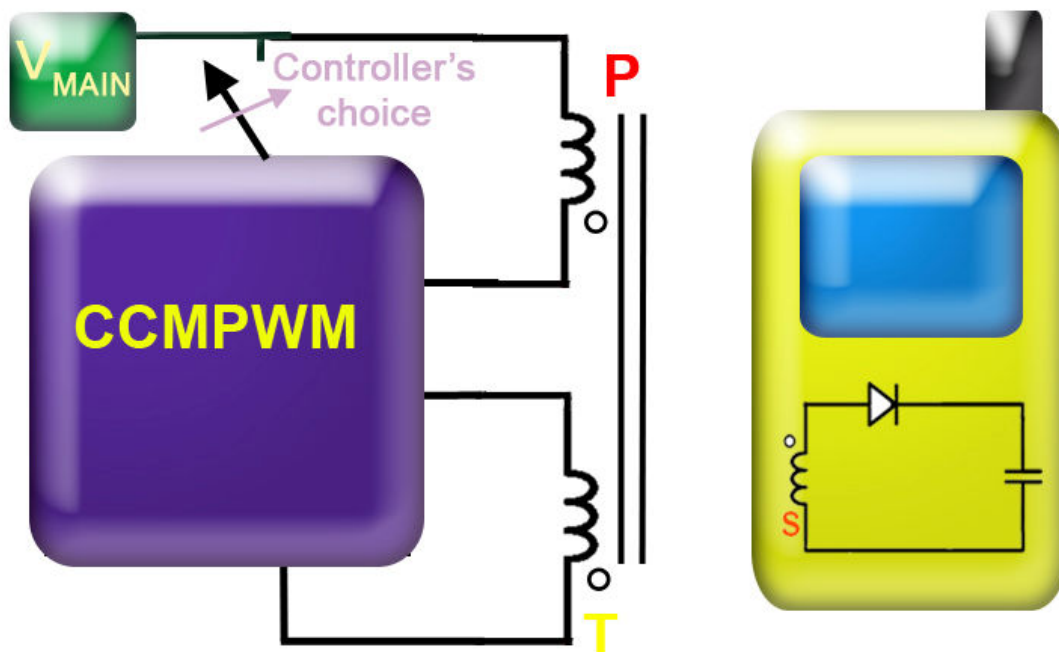
Figure 2: Simple sketch of the system

As shown in Figure 2, the basic structure of the system can be divided in two main parts. The primary arm, P, of the transformer generates a magnetic field with the energy from an external power supply. The controller regulates the output by switching between ON and OFF according to what is sensed through the Tertiary arm, T. This switching decision is made by a Current-Mode Pulse Width Modulator Controller (CCMPWM). Because a varying current through a coil results in a voltage according to equation (1) and this change in voltage

is mirrored at each of the coils (each with its specific inductance L) composing the transformer.

$$V_L(t) = L \frac{dI_L(t)}{dt} \qquad \text{(1)}$$

Because the secondary side of the transformer, S, is placed inside the handheld device, it will only take energy from the field produced by the primary when it is close to the primary coil.

3. Method/approach

Before modelling, a real device was selected from the available choices of current controlled pulse width modulated controllers in the market in order to have a clear idea of what was necessary to simulate. The **MAX5068E** [15] from Maxim Integrated Products, Inc. was chosen for the system implementation because:

- It is a low cost readily available, current mode pulse width modulator controller.
- It is well suited for universal input (i.e., from any standard power mains supply), so it can handle high voltages, essential for this application.
- It allows switching frequencies ranging over **12.5..625 KHz,** which are high enough for the correct functioning of the magnetic field coupling through the transformer.
- It provides a SYNC input for synchronization to an external clock (making it easy to turn **the device ON** when another device with a secondary coil is over this specific primary coil in an array, such as might be placed at a turnstile).
- It has a **programmable** internal slope-compensation circuit which is used to stabilize the current loop; it operates at duty cycles over 50% (its maximum Duty Cycle is 75%): Instead of using this for regulation, it will be used to *"fool"* the circuit so as the maximum power is transfered to a supercapacitor placed at the secondary side of the transformer (this will be broadly explained in section 3.1.2.)
- It is a low cost chip (<US$2) and it uses a tiny surface mount device package so that arrays of these devices and coils can easily and cost effectively be built

3.1. The configuration: Basic Parts, Functioning.

As marked on Figure 3, there are a number of pins with various functionalities to control an SMPS built with this CCMPWM. A detailed description of the pin functionality follows.

3.1.1. V_{IN}

As high as possible to maximize the power injection into the circuit (P~V x I) while maintaining reasonable component voltage ratings.

3.1.2.   Reservoir capacitor

C1 should be at least 100 μF (the value specified in the datasheet as typical) because it must be big enough to store enery during the 2047 T_{CLK} cycles that the circuit's soft-start lasts.

3.1.3. Buck Regulator

The chip controls NDRV to switch Q1 between ON/OFF, while the energy is stored at the reactive elements (in this case the transformer coils) during the ON states and smoothly supplied during the OFF states, guaranteeing a regulated output. As seen from the theory regarding SMPS:

$$L \times I_L = \frac{V_{ON} \times D}{r \times f} = \frac{V_{ON} \times D}{f} \times \frac{1}{r} = \frac{E \times t}{r} \quad \text{(2)}$$
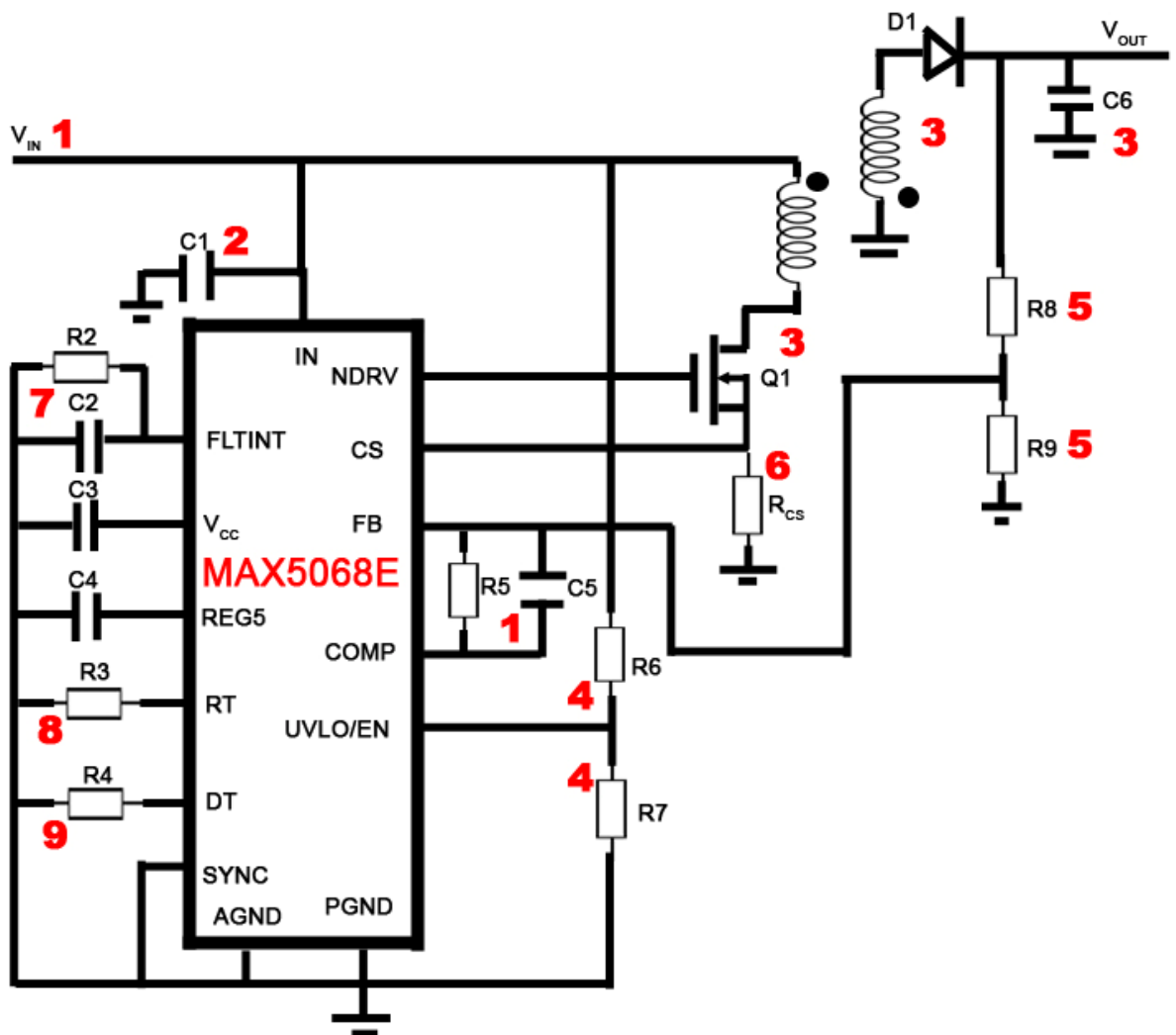
Figure 3: MAX5068E on the initial configuration

Since it is a *Buck regulator* where:

$$I_O = I_L \quad \textbf{(3)}$$

$$L = \frac{V_{ON} \times D}{r \times f \times I_O} \quad \textbf{(4)}$$

And where $V_{ON} = V_{IN} - V_{OUT}$, D = Duty Cycle established at 75% maximum, r = 0.4 (rule of thumb for the design), f = f_{SW}. For more information see appendix A.

The inductance of the transformer windings are a function of the number of turns, the dimensions of the coil, and the material of the core as shown in equation 5.

$$L = \frac{\mu_0 \mu_R N^2 A}{l} \quad \textbf{(5)}$$

μ_0 is the permeability of free space ($4\pi \times 10^{-7}$ H/m)
μr is the relative permeability of the core (dimensionless)
N is the number of turns.
A is the cross sectional area of the coil in m²
l is the length of the coil in m
i is the current in A

Equation 6 gives the flux density.

$$B = \frac{Li}{NA} \quad \textbf{(6)}$$

3.1.4.   Reference Voltage Regulation Loop

$R_{HYST}=0$ (not shown in Figure 3 because the HYST pin is not available on the MAX5068E, *the model of the device that is used*) this means that the voltage indicating the change of cycle is the same to switch from ON→OFF as to switch from OFF→ON) **R6** and **R7** constitute a voltage divisor that will present at UVLO/EN the voltage indicating when NDRV should switch, hence causing the transistor to change between ON or OFF. Thus, in a SMPS R6 and R7 are calculated to achieve a desired V_{OUT}.
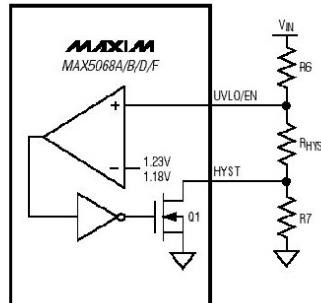
Figure 4: UVLO/EN regulation circuit (appears here with the permission of the copyright owner)[15]

- When UVLO/EN rises over 1.23V, Q1 is turned ON by means of NDRV.
- When UVLO/EN falls under 1.18V, Q1 is turned OFF by means of NDRV.

As a result regulation is achieved by switching between two states where the reactive elements charge/discharge alternate creating a smooth energy flow at the output provinding feedback information.

$$R6 = \left(\frac{V_{ON}}{V_{ULR2}} - 1\right) \times R7 \qquad (7)$$

In equation 7, $V_{ON} = V_{IN} - V_{OUT}$; V_{ULR2} = UVLO/EN rising threshold = 1.231V

3.1.5.   Internal Error Amplifier

R8 and **R9** constitute a voltage divisor of V_{OUT} providing an **input to pin FB with a voltage proportional to V_{OUT}.** This voltage divisor is the key regulating the output, where the voltage level is chosen to provide FeedBack, FB. On top of that, by controlling the relation between these two resistors, it is establishes the voltage which the output will be regulated to.

$$V_{OUT} = \left[\left(1 + \frac{R8}{R9}\right) \times V_{REF}\right] \qquad (8)$$

In equation 8, V_{REF} = 1.23V

The slope compensation internal circuit generates a ramp whose slope is determined by SR (see equation (9)) at f_{SW} which is added to the current sensed through CS and compared with the output of the error amplifier, COMP, to decide whether NDRV should continue conducting after the initial spike or not.

The reason for adding this sawtooth whose frequency is the same as f_{SW} to the current sensed is to increase stability and avoid oscillations:

   "Ridley demonstrated that the Q becomes infinite at D=0.5 with no external ramp, which confirms the inherent instability of a current mode SMPS which has a duty cycle greater than 0.5."[25]

$$SR = 90mV/\mu s = \frac{165 \times 10^{-6}}{R_{RT} \times C_{SCOMP}} = \frac{N_S \times K \times R_{CS} \times V_{OUT}}{N_P \times L} \qquad (9)$$

In equation 9, N_P and N_S are the number of turns at the primary and secondary side of the transformer (in our application, $N_S \ll N_P$), K = 0.75, L is the secondary filter inductor (whose value depends also on N_S); V_{COMP} is in the range of [0.4V, 1.1V] in the Low (OFF) case or V_{COMP} is in the range of [2.6V, 3.8V] in the High (ON) case, thus the output voltage of the internal error amplifier is minimized when V_{OUT} reaches the desired value.

3.1.6. Current Sensing through the Primary Arm of the Transformer

R_{CS} presents a voltage input to current sense, CS, proportional to the current flowing through the primary arm of the transformer.After adding this to the slew rate, SR, the sawtooth waveform is compared at the pulse width modulator, PWM, comparator with the error amplifier output, to determine if NRDV should be switched off:

$$I_{PRIMARY} \times R_{CS} > (V_{EA} - V_{OFFSET} - V_{SCOMP}) \qquad \textbf{(10)}$$

Equation 11 is used to limit the maximum current at the primary:

$$R_{CS} = \frac{V_{CS}}{I_{PRI}} \qquad \textbf{(11)}$$

In equation 11, V_{CS} = 314 mV; I_{PRI} = $I_{PEAK\ @\ PRIMARY\ CIRCUIT}$

3.1.7. IC protection against transient overcurrents

$$C_{FLINT} = \frac{I_{FLINT} \times t_{SH}}{2.8} \qquad \textbf{(12)}$$

$$R_{FLINT} = \frac{t_{RT}}{0.595 \times C_{FLINT}} \qquad \textbf{(13)}$$

In equations 12 and 13, t_{SH} = Shutdown time of the circuit, I_{FLINT} = 60 µA, t_{RT} = 10 x t_{SH}

3.1.8. Switching frequency (f$_{SW}$)

$$R_{RT} = \frac{10^{11}}{4 \times f_{SW}} \qquad \textbf{(14)}$$

The switch will turn ON at the beginning of each cycle, creating at least, spikes at a rate indicated by f_{SW}. Equation 14 described how resistor R_{RT} determines this frequency.

The MOSFET can either keep on conducting current during, **at maximum,** the time indicated by (Duty Cycle)*T_{CLK} or not. It will not conduct if V_{OUT} is high enough or there is too much current flowing through the coil (measured by CS) or other exceptions like Thermal Shutdown, Digital Soft-Start or Dead Time (will only turn it off after conducting during a whole duty cycle).

Figure 5: NDRV ON at 75%Duty Cycle (left); spikes when NDRV should be OFF (right)

3.1.9.   Dead Time: Duty Cycle time decrease

R_{DT} can be used to slightly decrease the time of the maximum allowed Duty Cycle (in any case, it will never be greater than 75% of T_{CLK} ON) to prevent transformer saturation at the primary side. This is established by the Dead Time as described on equation 15:

$$DT[ns] = \frac{60 \times R_{DT}[k\Omega]}{29.4}$$ **(15)**

3.2. Topology modifications: From suggested to desired implementation and function.

In this study a **separable** SMPS is required as a basic component. So, there cannot be any control loop directly connecting the energy buffer output with the controller, i.e., without using a wire or another connection i.e. LED + Optical Sensor. Otherwise the mobile device would need to be tethered in some way to the controller. This separable solution based on a transformer[16] is shown on Figure 6:

$$\frac{V_P}{V_S} = \frac{I_S}{I_P} = \frac{N_P}{N_S}$$
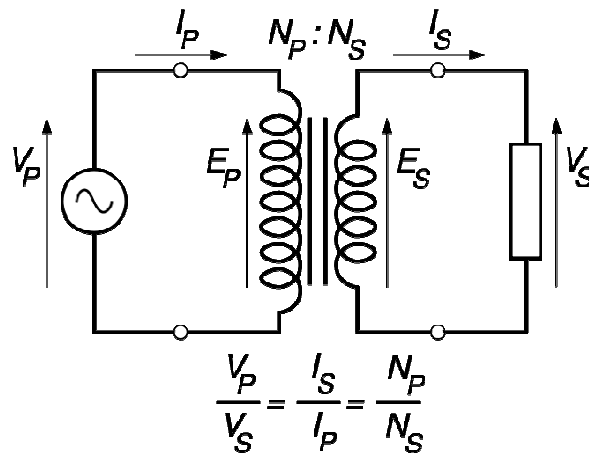
Figure 6: Ideal transformer behavior [16]

Current will start flowing when a load is placed at the secondary. This current will generate a magnetomotive force over the secondary winding that will oppose the primary. As a result, the flux on the core will be reduced [17]. Since this flux decrease will also reduce the back electromotive force, emf and disturb the equilibrium of the primary circuit [18] the current in the primary will rise, increasing the core flux until the supply voltage is again matched and the effect of the energy taken from the secondary will be compensated for [19]. Consequently, the core flux and both primary and secondary emfs remain the same, regardless of the secondary current, as they are determined only by the voltage at the primary side of the transformer. Therefore energy fed into the primary is transferred to the secondary. [16]

This behaviour of transformers is exploited as shown in Figure 8 to form a separable circuit while maintaining proper closed-loop operation of the controller by adding a tertiary winding to the transformer permanently co-located with the primary winding. The tertiary winding will cause the controller to attempt to maintain proper closed-loop operation regardless of the location of the secondary. The secondary is usually absent, and only sometimes placed close enough to collect magnetic field lines and therefore, energy; this balance (or imbalance) (between *supplier* and *consumers* of energy) would appear, at the same time in the secondary and tertiary:

- Secondary away: The controller switches NDRV between ON/OFF to mantain a constant average V_{OUT} as sensed through the FB path. The energy consumed by the load on V_{out} is simply wasted energy.

- Secondary on top of the primary (and tertiary): When the secondary coil approaches, magnetic flux coming out of the primary half-core will go into the secondary, generating a magnetic flux there, thus energy will be transferred in this way from the primary to the secondary coil. Additionally, more energy will be supplied by the primary until the V_{OUT} (sensed as the output the load by the tertiary coil, placed in the fixed part of the circuit), sensed as FB (as before), results in a regulated voltage value. This means that during the imbalance the secondary rapidly receives power from the primary, until the tertiary is back in regulation, at which point the secondary reaches

10

a voltage which is is proportional to the voltage on the tertiary (in proportion to the number of windings, assuming that the cores are the same diameter and aligned). This occurs because when back in regulation the ratio of voltage in the primary and tertiary is proportional to the number of turns about the primary and tertiary, which are ideally always aligned.

In other words, **the effect of the** *load* (in this application, a **capacitor buffering energy**, placed inside the handheld device and attached to the secondary) will **show up at the tertiary arm (that also has a load)**, in the fixed part of the circuit, **as a result of magnetic coupling, without** requiring **any other** kind of **connection**.

It's known that the effective impedance of a capacitor varies even while being charged to a constant DC voltage. It draws more current at the initial stage. There is no strict regulated source requirements in order to place energy into the buffer so the variations in the current while the capacitor is charging and while the SMPS is trying to bring the output back into regulation (based upon FB) will not damage the capacitor, as long as the voltage across the capacitor voltage is less than or equal to its voltage rating.

$$V_C(t) = V_{DCSOURCE} \times \left(1 - e^{\frac{-t}{RC}} \right) \qquad \textbf{(16)}$$

$$i_C(t) = C \times \frac{dV_c(t)}{dt} \qquad \textbf{(17)}$$

The behavior of a capacitor charging from an ideal independent voltage source ($V_{DCSOURCE}$) is shown in Figure 7 and described by equations 16 and 17. **In this solution $V_{DCSOURCE}$ is dependent** because of the closed-loop nature of the controller. Therefore the shape of the capacitor charging curve using the circuit described in Figure 8 will deviate from the ideal. This is described in detail later in the thesis.
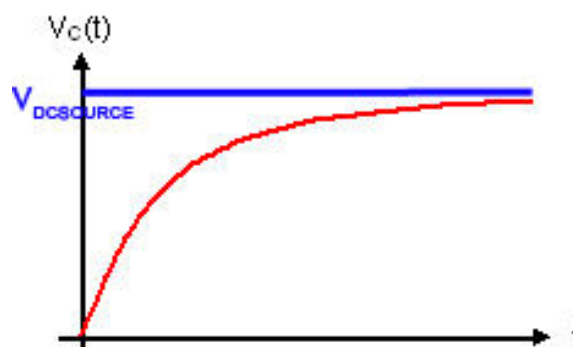
Figure 7: Capacitor charge through a RC series circuit
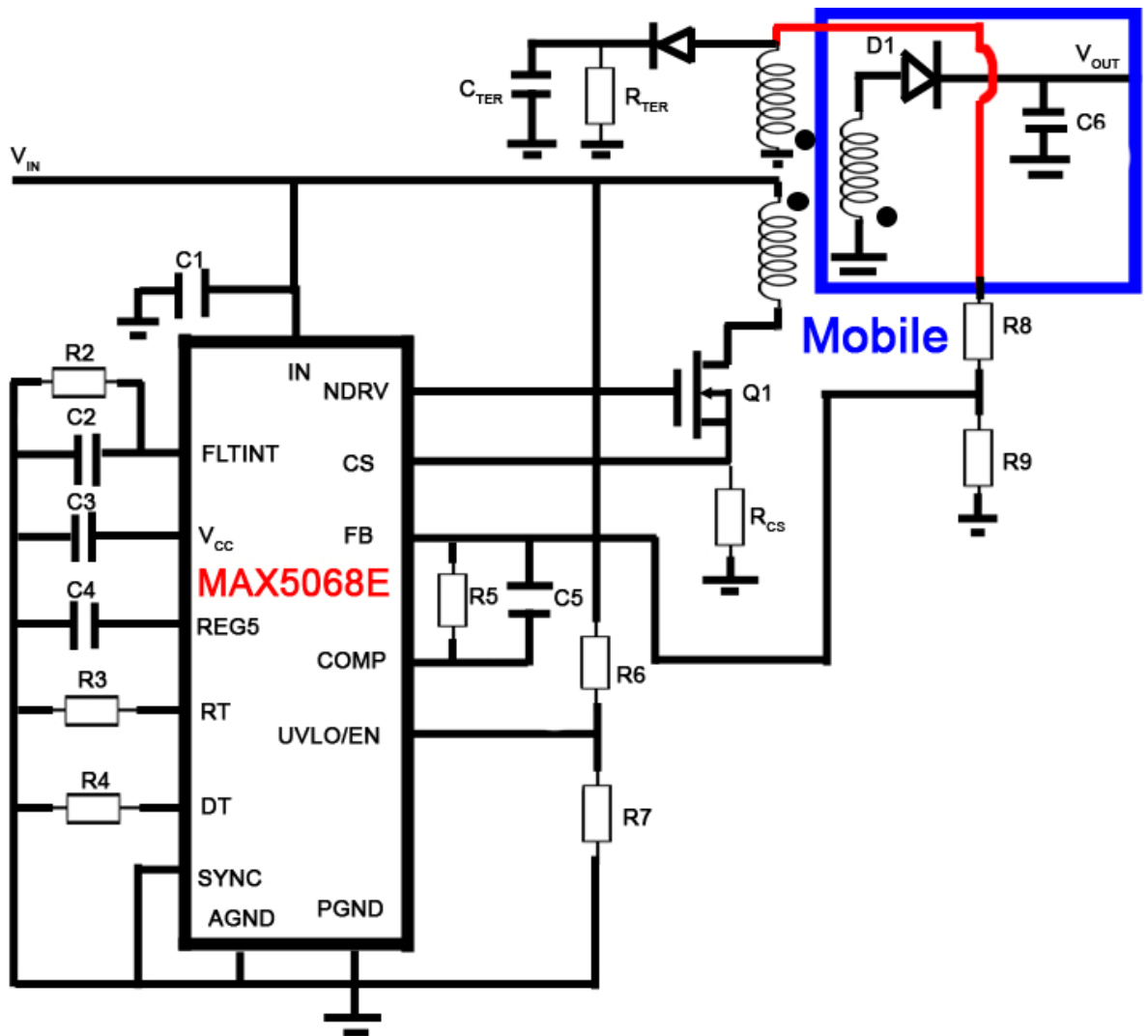
Figure 8: Initial suggested configuration

4. Computer Model of a generic SMPS

4.1. Choice of Simulation Environment

As stated before, the purpose of this study is to transfer energy through magnetically coupled coils via an inductive field in the Near Field zone, which could occur while sliding one secondary coil past an array of other primary coils. The energy is to be transferred to a secondary coil where it will be buffered on a capacitor in order to supply power to a mobile device. As part of this project we want to design, optimize, measure, and evaluate a single cell of such an array of primary coils. One of the best ways of designing and optimizing any circuit is to build a detailed model where element values and/or topologies may be easily modified. Additionaly, there is no risk of hurting anyone by using high voltages, as might

occur when experiments are performed to determine where the physical limits are. The modelling language used is a modified version of SPICE [20] [21]. Although SPICE has a long history of use for integrated circuit design, it is unable to simulate hybrid (analog-digital) circuits simultaneously nor to simulate magnetic hysteresis (nonlinear magnetic core behavior) [24]. However, the later is present at the transformer with a ferrite core (which has been used to increase the magnetic field intensity) through which the coupling between primary and secondary sides is done. Literature research [25] was conducted to find a suitable simulation solution. This literature study uncovered Steven M.Sandler's, book "Switchmode Power Supply Simulation with Pspice and SPICE3" [25].

Pspice [26], allows advanced simulation of analog & mixed-signal environments. Initially this appeared to offer the best alternative, but after some difficulties finding a Linux version of PSpice, an open source software package for Linux, ngspice [27] was chosen. Ngspice contains Xspice [28] which supports the mixed-mode and non-linear simulation requirements. It is an extension to the SPICE3 simulator providing the ability to use code based models written in the C programming language to add new user-defined models when the element needed is not already implemented by the XSPICE model library. This library contains over 40 new functional blocks including summers, multipliers, integrators, magnetic models, limiters, S-domain transfer functions, digital gates, digital storage elements, and a generalized digital state-machine. How these models were used and extended is described in the next section.

4.2. Simulation Approach Method

Sometimes integrated circuit vendors provide SPICE models. While Maxim makes available many SPICE models, unfortunately they do not have one available for the MAX5068. This controller is the core of a Switching Mode Power Supply. Its purpose is the regulation of V_{OUT} by deciding when to switch the MOSFET between ON and OFF. The MAX5068 has high internal complexity, containing in addition to the basic regulation functions, a lot of extra circuitry intended to prevent damage to the IC and to control some internal functions not related to power supply operation. As it was not a concern of the thesis to consider all of these "corner" cases, the wisest option, rather than model the complete controller was to simply model its switch mode power supply behaviour, i.e. its regulation of the MOSFET during normal operation.

A literature study led to an article by Christophe Basso on writing models for power supply controllers [29]. Even if architectures for SMPSs are complicated, such as the one for the MAX5068 as shown in Figure 10, the core functionalities are the same. The secondary functions (such as the pins and functional units used to supply the chip with regulated power or the control loops to protect them against overcurrent situations) can be optionally modelled. By only modelling the core funtionalities, a very simple model of such a current control pulse width modulator controller (shown in Figure 9) can be used in a XSpice circuit description. This model leads to a very simple suggested circuit realization, shown in Figure 10.
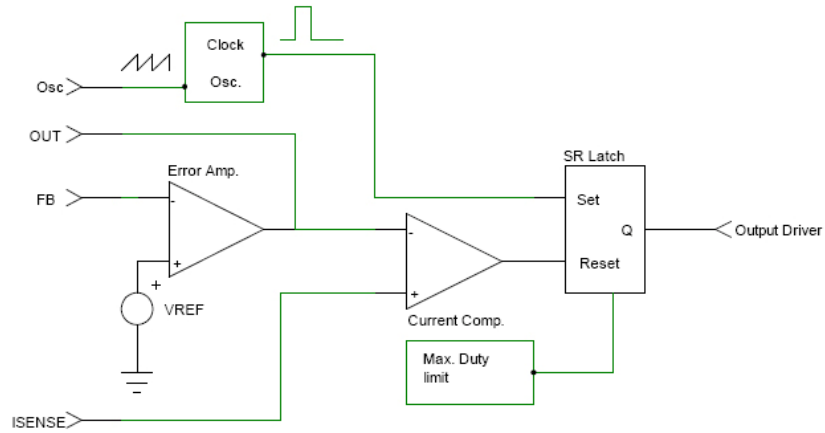
Figure 9: The internal circuitry of a generic single output CCM PWM controller [29]
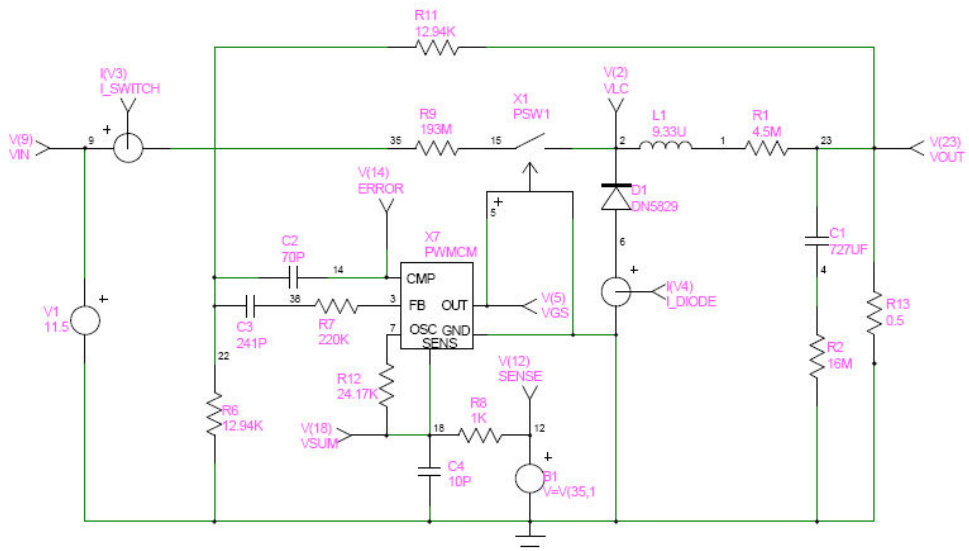
Figure 10: Suggested architecture for a current-mode controlled Buck regulator (see appendix A.2.1. for more information about Buck regulators) [29]
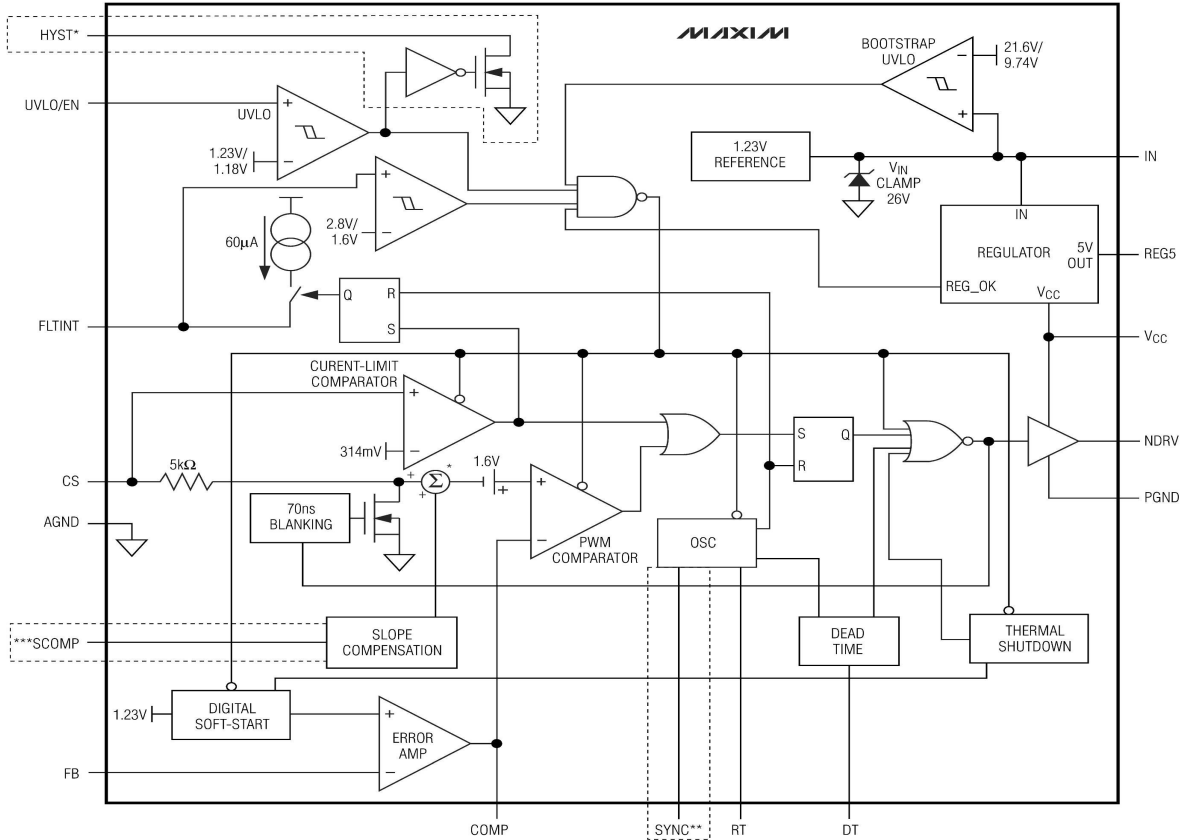
Figure 11: Internal MAX5068 configuration (with permission from the copyright owner)[33]

Comparing Figure 9 and Figure 10 with the internal block of the MAX5068 shown in Figure 11 a number of equivalences can be seen.

- The **PWM COMPARATOR** is the current limit comparator between the voltage generated by the current through CS ($I_{CS}xR_{CS}$) and the output of the Error Amplifier, called the Current Comparator in the simplified model. Therefore, **CS** of MAX5068 is the equivalent pin to ISENSE here.
- The **Error Amplifier** with feedback is the same in both. V_{REF} in the generic model is fixed at 1.23V in the MAX5068.
- The pin named **NDRV** used to switch the MOSFET of the SMPS between ON/OFF is more or less the same as the Output Driver of the generic model (more signals are taken into account in the MAX5068, because it is a more complex circuit which includes several more control loops). In the generic model, the Output Driver is turned OFF when the current coming from ISENSE is greater than the output of the error amplifier (coming from the comparison between Vref and FeedBack voltage) the functioning is exactly the same in MAX5068. However, in order to see it clearly it should be noted that even though

15

connections are done in the opposite way, there is a NOR logic gate which will turn the latch OFF whenever one of the inputs (no matter which) is '1'.
- **SYNC**, providing synchronization to an external clock is the equivalent to the ENABLE pin.
- **COMP** of the MAX5068 is the equivalent to OUT in the generic model, this is only a control pin to reveal what is happening at the output of the Error Amplifier.

Even if the suggested architecture for a SMPS using the MAX5068 datasheet may seem more complicated, the primary differences are the result of supplying the circuit with DC power that involves pins IN & REG5 as well as the functional unit REGULATOR. The generic model has no equivalent, as it simply assumes that there is suitable available power supply for the controller itself. Finally, UVLO/EN programs the input-supply STARTUP voltage and ensures proper operation during brownout conditions. This circuit also has no equivalent in the generic model, because the model has assumed that there is always sufficient power coming into the device. The OSC signal in the simplified model is simply a ramp compensating signal. The MAX5068 incorporates an adder to achieve slope compensation that is not included in the generic model of the CCMPWM, but implemented at node 18 in the circuit shown in Figure 10. This same approach is used in the circuit which was built and simulated, thus the ISENSE (pin 18 in Figure 10) comes from the addition of the slope and the current sensed. However, this is done outside of the controller in the simplified model.

Many elements of the MAX5068 were simply removed because they had no relevance at this stage in the modelling. For example, DT only provides a small adjustment of the Duty Cycle. FLTINT provides a protection to ignore overcurrents in case they happen during a short period of time and RT is simulated in SPICE using a clock. Hysteresis, HYST, is not available on the version E of MAX5068 which is used in this application, hence it was not modelled. UVLO/EN is used at the start-up of the circuit as well as a protection to allow self-functioning even in brownout cases, therefore was not included in the simulated circuit. Note also that, in the real circuit, if VIN drops below 9.74V, then a Digital Soft-Start ("reboot" of the circuit) is done through node {1} on Figure 8. Even though this regulation is necessary, these elements were omitted at this stage of modelling.

As shown on Figure 11, an internal clamp circuit is used to prevent the bootstrap capacitor C1 (depicted in Figure 8) from charging from a voltage beyond the absolute maximum rating of the device when UVLO/EN is low (device is in shutdown). Additionally, if the temperature exceeds some limit, then the circuit is also turned off. Finally, REG5 may also be substituted by a 5V/18mA source while V_{CC} and PGND are used by the front end amplifier to increase the level of the ON/OFF voltage to sufficiently high for driving the MOSFET of the SMPS circuit ON/OFF. It is not necessary to include these in the SPICE model. The "70ns Blanking" is only used if CS is above the maximum current limit, when the transistor is driven ON, and the voltage added to the slope compensation goes rapidly to 0 to compensate for this overcurrent (when there is a '1' at the output of the Current Limit Comparator, then there is a '1' at the output of the OR gate, the Latch has a '1' in Set so its output Q goes to '1' fastly turning the NOR output to '0' starting the 70ns blanking. These functions were not included in the SPICE model.

5. Hardware Implementation

5.1. Hardware Design

As soon as the feasability and convergency of the system was established by the SPICE model (see section 4), the next was to design and build the real circuit. Using the MAX5068 datasheet specific components for the design were determined. A Microsoft EXCEL spreadsheet was used to facilitate easily changing values in order to explore the design space. Using a spreadsheet allowed all dependent values to be automatically calculated.

Table 1: Initial components calculation

	Expression	Theoretical Value	Actual Value	Units
f_{SW}	$10^{11}/4*R_{RT}$	2,00E+05	2,08E+05	Hz
t_{DT}	$60*R_{DT}[k\Omega]/29.4$	7,96E+02	7,96E+02	ns
t_{RT}	$10*t_{SH}$	4,70E-02	4,70E-02	s
t_{SH}		4,70E-03	4,70E-03	s
T_{CLK}		5,00E+00	4,80E+00	µs
D		5,00E+01	5,00E+01	%
T_{ON}	$T_{CLK} * D$	2,50E+00	2,40E+00	µs
I_{FLINT}		6,00E+01	6,00E+01	µA
N_S		20	20	turns
N_P		20	20	turns
I_{PRI}	$I_{LOAD}*N_S/N_P$	I_{LOAD}	I_{LOAD}	A
r		4,00E-01	4,00E-01	
L	$V_{ON}*D/r*I_{LOAD}*f_{SW}$	25	25	µH
SR	$165*10-6/R_{RT}*C_{SCOMP}$	2,00E+01	2,00E+01	mV/s
VREF		1,23E+00	1,23E+00	V
VIN		2,00E+01	20	V
VOUT	$(1 + R8/R9)*VREF$	1,20E+01	1,58E+01	V
VON STARTUP		1,00E+01	1,00E+01	V
VULR2		1,23E+00	1,23E+00	
VON	VIN - VOUT	8,00E+00	2,00E+01	V
C1		1,00E+00	1,00E+00	µF
CFLINT = C2		1,00E-07	1,00E-07	F
CVCC = C3		1,00E+00	1,00E+00	µF
CREG5 = C4		1,00E-01	1,00E-01	µF
CSCOMP = C7	165*10-6/RRT*SR	6,60E-11	6,88E-11	F
C6		NP	NP	
R1		2,20E+02	2,20E+02	kΩ
RFLINT = R2	tRT/0.595*CFLINT	7,90E+05	8,20E+05	Ω
RRT = R3	1011/4*fSW	1,25E+05	1,20E+05	Ω
RDT = R4		3,90E+02	3,90E+02	kΩ
R5		3,90E+02	3,90E+02	kΩ
R6	(VON STARTUP/ VULR2 -1)*R7	1,92E+02	1,80E+02	Ω
R7		2,20E+04	2,20E+04	Ω
R8	(VOUT/VREF - 1)*R9	1,93E+05	3,90E+05	Ω
R9		2,20E+04	3,30E+04	Ω
RCS	314[mV]/IPRI[mA]	5,00E-02	5,00E-02	Ω

5.2. Hardware Construction

The final circuit was implemented as a circuit board. In order to do this implementation a number of tools were used, each of these is described below.

- CAD Tools

OrCAD®Capture [31] was used for design capture and to generate a suitable NetList which was converted, with the help of OrCAD®Layout [32], into a single-sided circuit board to which all the components were soldered.

- Design Capture

The initial circuit as captured is shown in
Figure 13. Some extra-components which appear as NP (Not Populated) were placed between strategical nodes, to simplify future modifications.

- Layout

Figure 12 shows the bottom board view. Here the traces between components (red, indicating bottom layer), as well as their padstacks (the surface mounted devices padstacks on the bottom layer are shown in red; while the through hole padstacks on the top layer are shown in pale blue). Yellow marks the outline of the board, in order to separate this board from others which might be on the same panel.

Except for the MAX5068E and R$_{CS}$, all the remaining components are mounted through the board.
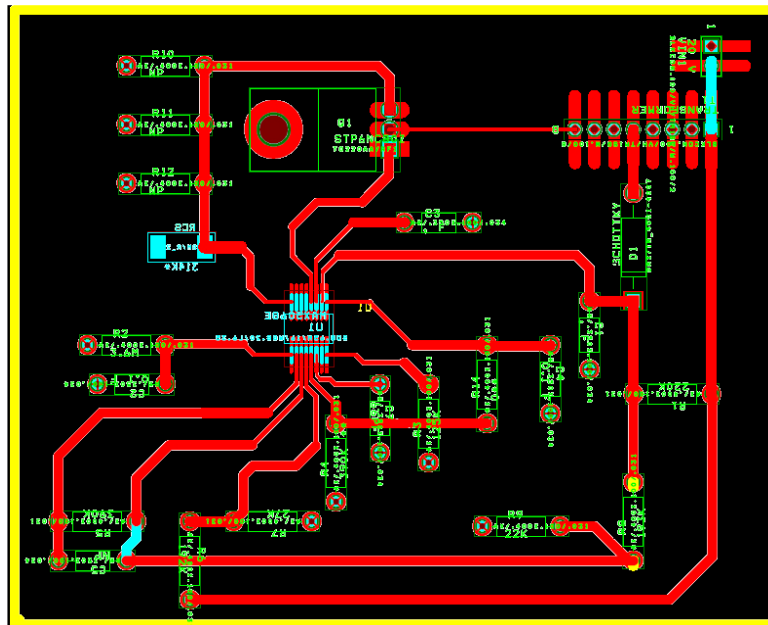
Figure 12: PCB footprint

- Board Fabrication

Post processing of the layout files generates Gerber files which are used to fabricate the board (i.e., the spatial placement of the actual layout onto the circuit board material). These Gerber files are used by a circuit board milling machine [51] to create a single instance of the circuit board, by removing copper from places where there should not be connectivity. After the circuit board was milled and separated from the panel, then components were soldered on.
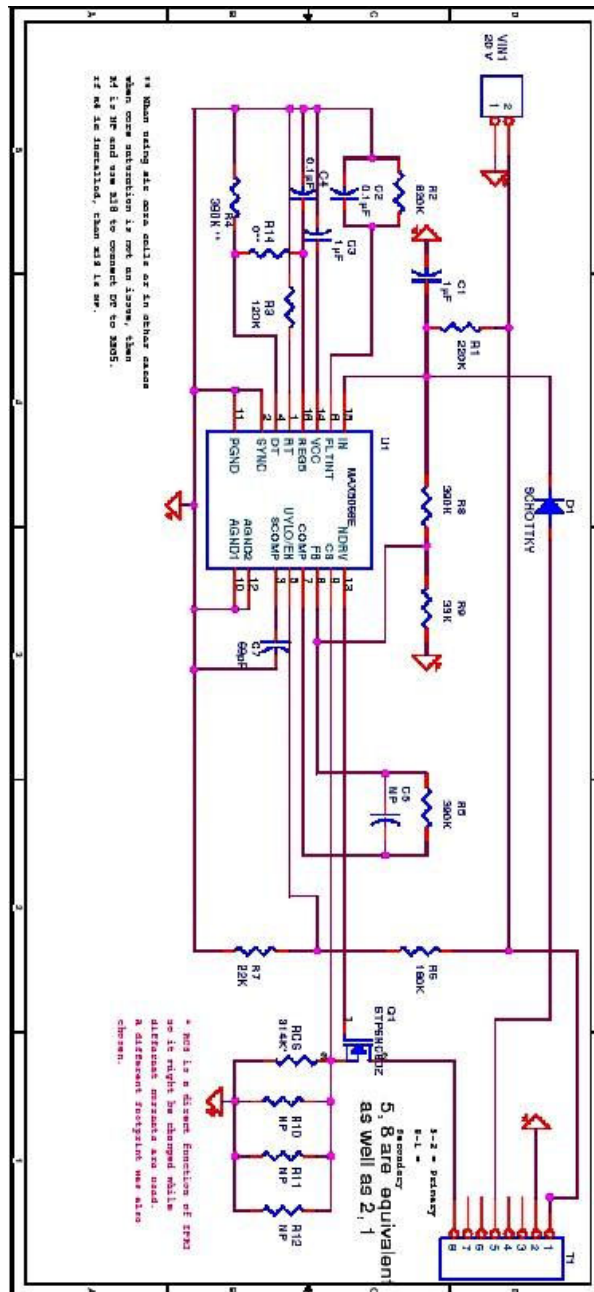
Figure 13: Initial Design

5.3. Hardware Refinements

5.3.1. Initial Tests

The design previously described had some parts changed and some additions made in order to prevent the MAX5068 chip from being damaged. First, the supply voltage V_{IN} was reduced from 20V to 12V while the transformer (primary and tertiary) was built by winding copper wire around a toroidal core (note that this toroid had not yet been split into to two physically separate parts) and the trace joining the node where the diode and R8 went into the IN pin was cut and a wire placed between the external DC source and the IN pin in order to make sure that the MAX5068 gets 12V DC to operate and the output regulated voltage value was decreased from roughly 16V to 9V by changing the values of R8 and R9 (they had been calculated to give 1.23V at FB pin when V_{OUT} equaled roughly 16V, to give the desired new output voltage the parts were changed to: R8 = 220K; R9 = 33K in order to achieve V_{OUT} = 9.4V). Finally, a load was connected to the diode, R8, and R9, consisting of a 47 µF capacitor in parallel with a 12V bulb. This is to simulate a load and to have a visual output that things were working correctly.

The power source was then turned on, the voltages in some of the pins (REG5, VCC) had their expected values and the chip was not warm, FB had a dramatically low value, while (as it was logically expected) COMP was very high, indicating the absence of regulation at the output, however, **V_{OUT} didn't reach the desired level.**

5.3.2. Feedback from these initial tests, resulting design modifications

Some problems were detected and fixed. Each of these problems is described below along with the solution to this problem.

Problem #1: NDRV pulse width

During testing it was observed that NDRV showed **too narrow pulses.** After examining the datasheet again it was seen that:

> "*When the voltage produced by the current at the primary side of the transformer (which also flows through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (NDRV) quickly terminates the current on-cycle. In most cases, a **small RC filter is required to filter out the leading-edge spike on the sense waveform.** Set the corner frequency to a few MHz above the switching frequency.*" [33]

Therefore an **RC filter**, which works as a low pass filter, widening these spikes into longer pulses was placed at pin NDRV to fix the problem:
- **f_{CORNER} = 3.78 MHz (above the 300 KHz desired operating f_{SW})**
- **R_{FILTER} = 1.2KΩ**
- **C_{FILTER} = 220pF**

Problem #2: FB path

The internal connection and behaviour of FB (linked to the error comparator) was unclear from the documentation, neither information about the input impedance nor about leakage currents or voltages were given on the datasheet. As a result of such an incomplete description from the vendor and, in order to ensure a voltage at the input of the error amplifier, in other words, V_{FB} that reflected what was happening at the *output* (47µF in parallel with 12V bulb) the values of R8 and R9 where reduced while an extra resistor was placed series with FB. Now, most of the current flowed through R8 and R9 while only voltage information was passed through FB. R5 was also modified to 1M, leading to a gain on the Error Amplifier (error AMP) of -17.8.

Table 2: Modifications ensuring FB to receive a correct value

R5	1M
R8	8.2K
R9	2.2K
R_{FB}	56K
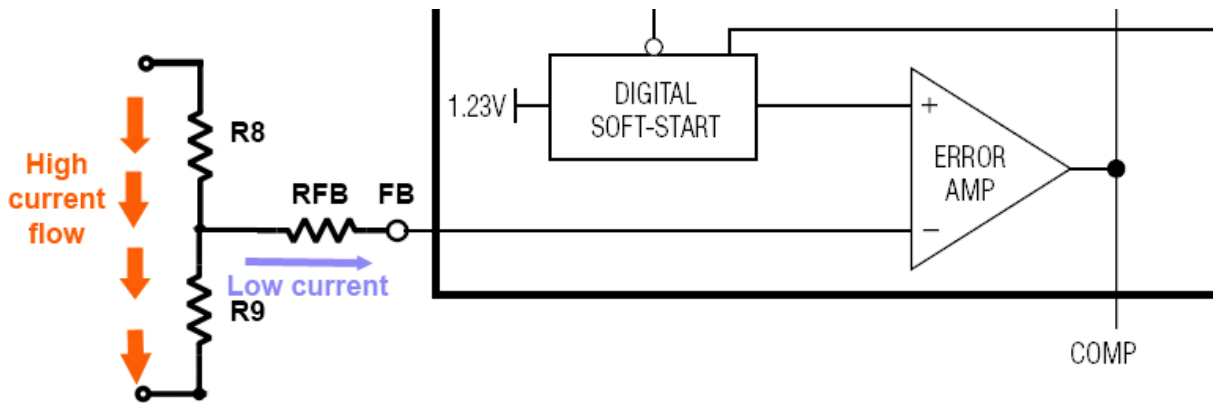
Figure 14: New configuration for the FB path

R_{FB} was added to provide a reasonable input resistance to the error amplifier, and R8/R9 were adjusted to have a much lower resistance so they would not be loaded down by the error amp. It was suspected that the previous higher resistances for R8, R9, and the absence of R_{FB} resulted in the input to the error amplifier being loaded down to the point where the output of the amplifier railed (i.e., swung to its power supply voltage) and stayed there preventing its proper operation.

Problem #3: Duty Cycle Limit

As the output was not reaching a high enough voltage, in order to maximize the Duty Cycle, REG5 was shorted by using DT (this was done by removing R4 and replacing R14 by a wire).

Problem #4: Transformer Choice

From the MAX5068 datasheet [33] it is known:

$$\frac{N_S}{N_P} \times \frac{K \times R_{CS} \times V_{OUT}}{L} = SR \qquad \textbf{(18)}$$

For the initial design:
- K = 0.75
- SR = 20mV/µA;
- V_{OUT} = 12V
- R_{CS} = 0.05Ω

Where the slew rate, SR, is the slope of the sawtooth used to keep the system away from oscillations (commented in section 3.1.5.   Internal Error Amplifier Therefore, since N_S = N_P was the initial test coniguration a value of **L in the range of 20 µH** results from using equation 18. Even if that value does not need to be exactly the same as the transformer arm's equivalent inductance, it is a suitable starting reference point. Some toroid cores were removed from old power supplies (i.e., recycled). Unfortunately, there was no other available information than that they seem to be from AMIDON [34]. Fortunately, AMIDON gives specifications in their catalogue relating the dimensions of each toroid core with the number of turns around it to achieve a specific inductance. Hence the following procedure was used:

1. Measurements of the physical dimensions of the first core (inside diameter = 0.312; outside diameter = 0.500; height = 0.250), led to its identification as a **AMIDON FT-50A**.
2. Different numbers of turns were wound around it. Next, the inductance was measured with an RLC meter **¡Error! No se encuentra el origen de la referencia.** working at 1kHz: Even if f_{SW} is much higher (300 kHz) the number of turns hopefully will not need to be very high, so the difference in value of the parasitic capacitance between turns at different frequencies will be considered negligible.

These values were compared with the data given by the AMIDON catalog(see Table 3 and Figure 15) and deductions from these measurements were made.

Ferrite Cores
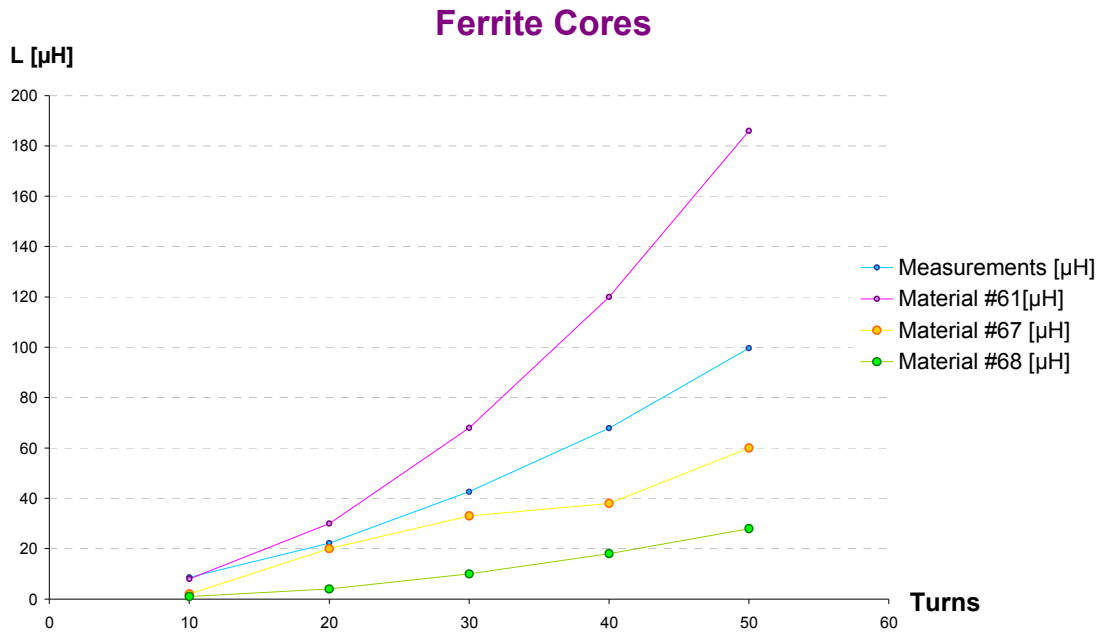
Figure 15: Graph comparing different materials and measured core behavior

Table 3: Comparing different materials (values from [34]) and measured core behavior

Turns	Measured [µH]	Material #61 [µH]	Material #67 [µH]	Material #68 [µH]
50	99,6	186	60	28
40	67,9	120	38	18
30	42,6	68	33	10
20	22,2	30	20	4
10	8,6	8	2	1

None of the values fit with what was given in the catalog, but a closer look at the graph shows that the measured material is something intermediate between materials #61 and #67. So even if the values relating inductance with turns are not given in the catalog, **material #64** [34] has a $\mu_{64\_MAX} = 375$; intermediate between $\mu_{67\_MAX} = 125$ and $\mu_{61\_MAX} = 450$. Therefore, our hypothesis is that the toroid was made of material #64.

3. 20 turns of wire were wound around the initial toroid core, giving a **L ≈ 25µH**; this was repeated to form both the primary and tertiary coils. Measurements of this configuration were used to **check the convergency and stability of the system**.
4. This test was **successful** with the voltage at the output regulated to 9V

Following the above test, a number of subsequent tests were made with other bigger toroids whose µ was determined to be much higher (estimated to be in the range of "*material J*"[34] or higher). Nevertheless, measurements revealed that in order to achieve a suitable L value

(within the range of 20-30 µH for the Primary and Tertiary as needed in order to keep the MAX5068 within regulation and avoiding problems with this chip) the number of turns should be very few, because a single turn led to 25 µH of measured inductance, while two turns produced 55 µH. Analysis of data from this trial showed that even if L has the same value, too few turns on the coil ruins the energy transfer by the transformer (i.e., between the primary and the secondary) so the voltage never rose to suitable levels with these cores. We would have predicted (using Faraday's law) that the emf would be proportion to the number of turns [35] and also because we know from equation 6 that the flux density, B, is directly proportional to the number of turns:

$$emf \propto N_{TURNS} \qquad \textbf{(19)}$$

Thus, it appears that there is a trade off between how high µ, the magnetic flux, and the inductive field can be while providing a good energy transfer. As no energy is stored in the transformer *forever*, thus what comes in when the switch (MOSFET) is turned ON will go out during OFF state. However, the construction which is exploited here is a Flyback Transformer, which stores energy in the air gap between both core halves - thus the amount of energy stored is related to the magnetic permeability of the air and the size of this gap.

These experiments gave a hint about suitable dimensions for N and µ; thus a relative magnetic permeability, μ_R, around 2000 was chosen, since it's high enough to avoid saturation, but not so large as to generate problems because of needing too few turns around the core. Such a material is material #77, which is also recommended by AMIDON for these applications [36]. Finally, a minimum N of 20 was determined after several tests, this allowed the load capacitor to charge and the system to perform as expected. The resulting new schematic is shown in Figure 16, and the new component values are shown in Table 4.
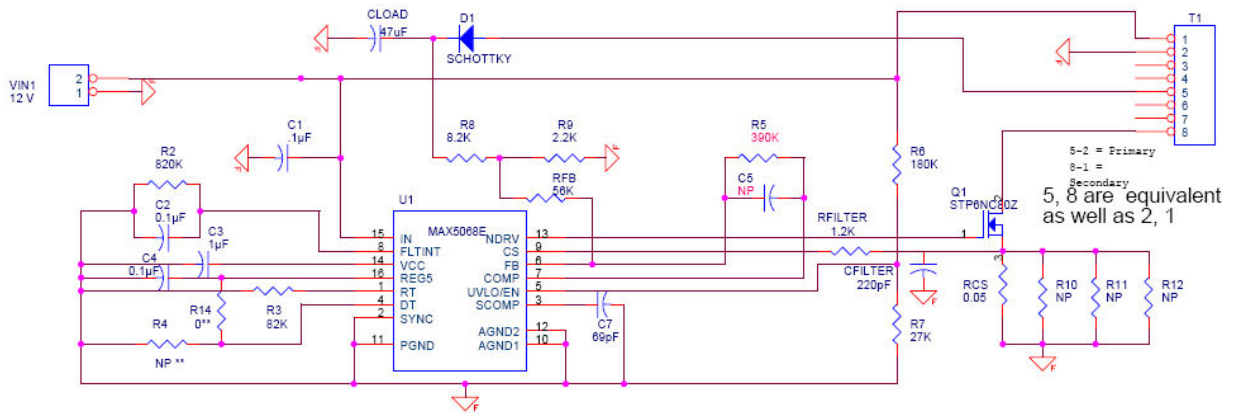
Figure 16: Capture Schematic of the refined circuit

Table 4: Refined component values

Parameter	Value	units
f_{SW}	304,88	KHz
C1	100,00	pF
C_{LOAD}	47,00	µF
Bulb	12,00	V
C_{FLINT} = C2	0,10	µF
C_{VCC} = C3	1,00	µF
C_{REG5} = C4	0,10	µF
C_{SCOMP} = C7	68,80	pF
C_{FILTER}	220,00	pF
R_{FILTER}	1,20	kΩ
R_{FB}	56,00	kΩ
R1	220,00	kΩ
R_{FLINT} = R2	820,00	kΩ
R_{RT} = R3	82,00	kΩ
R_{DT} = R4	390,00	kΩ
R5	390,00	kΩ
R6	180,00	kΩ
R7	27,00	kΩ
R8	8,20	kΩ
R9	2,20	kΩ
R_{CS}	0,05	Ω

The voltage at the output is given by equation 20:

$$V_{OUT} = \left(\frac{N_T}{N_P} \right) \times \left(1 + \frac{R8}{R9} \right) \times 1.17 \qquad \textbf{(20)}$$

The little 12V lamp placed in parallel with the 47µF capacitor joined to R8 and R9 started to light with this new configuration, and measurements with a volt meter showed a perfectly regulated voltage of 9V when the transformer was built by winding 20 turns in both, primary and tertiary sides around a toroid core with µ suspected to be material #64 from AMIDON [34], giving an approximate L of 25 µH.

5.3.3. System Startup

Once the tests showed regulation with the SMPS configuration similar to the simulation (see appendix B.3.), then it was time to add a third winding in order to start coupling energy into a secondary coil in a separate device (these results were expected to look like the final simulation shown in appendix B.4.)

The following convention will be adopted:

Primary [P]	Transformer arm placed at the fixed side of the SMPS that is connected to the MOSFET; it generates magnetic flux through the primary half of the ferrite core.
Secondary [S]	Transformer arm placed inside the handheld device that is connected to the load capacitor (probably a super capacitor) to draw energy from the magnetic field generated by P; this only occurs when this second half of the ferrite core is placed over the primary.
Tertiary [T]	Transformer arm placed at the fixed side of the SMPS that is wound around the primary half of the ferrite core, to draw energy from the magnetic field produced by P, in order to generate the FB voltage which is used to provide voltage regulation

The need for a separable core is the critical issue at this stage so P and T were wound around one of the halves of the core as part of the fixed part of the SMPS; while S was wound around another half of the core at the handheld device. Furthermore, previous results pointed out the approximate μ of the ferrite constituting the core, so this parameter was used to choose among the different options. Rather than attempt to cut a ferrite toroid, a pot-core which is already formed in two pieces was used. An example of such a split core is shown in Figure 17.

Figure 17: Pot-Core

Three different sized pot-cores were used to measure the inductance generated as a function of the number of turns, either when both halves are together or separated. Although there is an expression to calculate this inductance, as shown in Figure 18, the values were measured to achieve higher accuracy since the cores will never directly touch each other in our implementation.
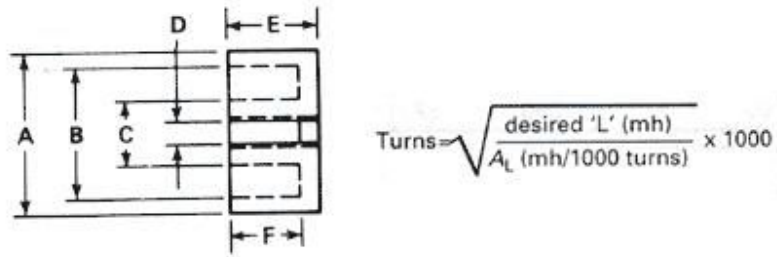
Figure 18: Dimensions and behavior of AMIDON's pot-cores

$$Turns = \sqrt{\frac{desired\ 'L'\ (mh)}{A_L\ (mh/1000\ turns)}} \times 1000$$

Table 5: Dimensions of the chosen cores

Core	Part Number	Physical Dimensions mm					
		A	B	C	D	E	F
SMALL	PC-1408-77	14.05	11.80	5.90	3.10	4.18	2.90
MEDIUM	PC-2213-77	21.60	18.70	9.25	4.55	6.70	4.70
BIG	**PC-2616-77**	**25.50**	**21.60**	**11.30**	**5.55**	**8.05**	**5.60**

Table 6: Magnetic Dimensions using the chosen cores (at f_{SW} = 20kHz). Subscript e indicates magnetic effective.

Core	Part Number	Magnetic Dimensions				
		A_e mm^2	L_e mm	V_e mm^3	A_L value mh/1000 turns	Max Power At 20 KHz
SMALL	PC-1408-77	25.0	20.0	500	1960	Max 5 watts
MEDIUM	PC-2213-77	63.0	31.6	2000	3660	Max 20 watts
BIG	**PC-2616-77**	**93.0**	**37.2**	**3460**	**4100**	**Max 50 watts**

Table 7: Different values for different sizes of Pot-Cores

Core	Turns	L_{WHOLE} [μH]	L_{HALF} [μH]
Big	6	27	5
	8	34	6
	20	**93**	**30**
Medium	10	35	6
	9	29	4.5
	8	24.5	3.7
Small	13	40	5.7
	12	30	5.5
	11	18	5.1

These values show that the inductance of one arm is a function of the separation of the pot-core halves; and the inductance increases as the separation decreases. This effect is

surprisingly suitable for the application, since when the handheld device is on top of the primary coil it will produce a higher magnetic field providing better energy coupling, while when nothing is on top of the primary, the SMPS simply generates a regulated V_{OUT}. Furthermore, a high L will not lead to damage because of the "Voltseconds Law" which states the higher the L, the lower the current as shown in equation 21.

$$L \times I_L = \frac{V_{ON} \times D}{r \times f} = \frac{E \times t}{r} \qquad \textbf{(21)}$$

To summarise, a **big core** with **20 turns** was chosen for the initial implementation of the separable system. After winding wires on both sides the following inductances were determined using ther RLC meter as described earlier.

Table 8: Values on the initial configuration

Side	Turns	L_{WHOLE} [µH]	L_{HALF} [µH]
Primary	20	92.7	31.2
Secondary	20	93	22.5
Tertiary	20	92.7	30

5.4. Hardware Tests / Data Collect

5.4.1. Experimental design

In order to provide a stable structure to place the fixed part of the SMPS (see Figure 19) so as to increase repeteability and reliability on tests, especially the final tests, when movement will take place, a rail of roughly 0.6m long was built (see the photographs in Figure 21). Note that the 12V bulb used as a load in the previous test (whose objective was to check the stability of the output voltage) was kept as visual *alarm* of something going wrong. Finally, to simulate the handheld device (see Figure 20), the secondary side of the transformer was placed inside the other half of the pot-core and was placed on a pad whose output was connected to an oscilloscope [51] to collect data. An extensive discussion of the oscilloscope data is given in section 6.2.
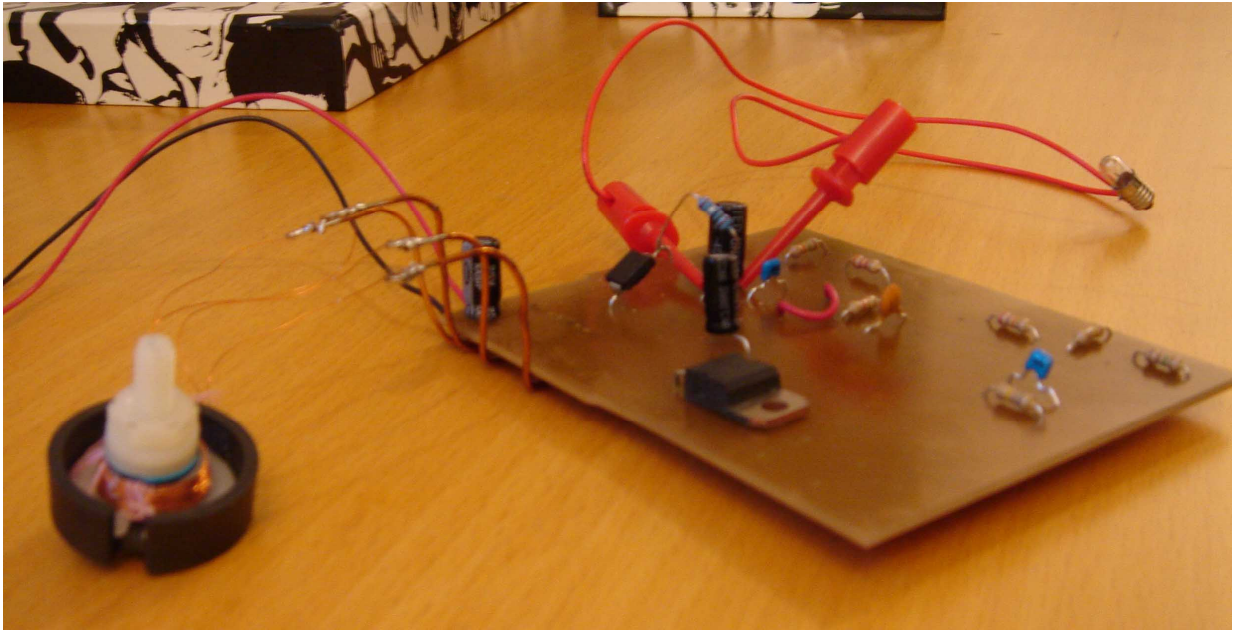
Figure 19: Fixed primary side
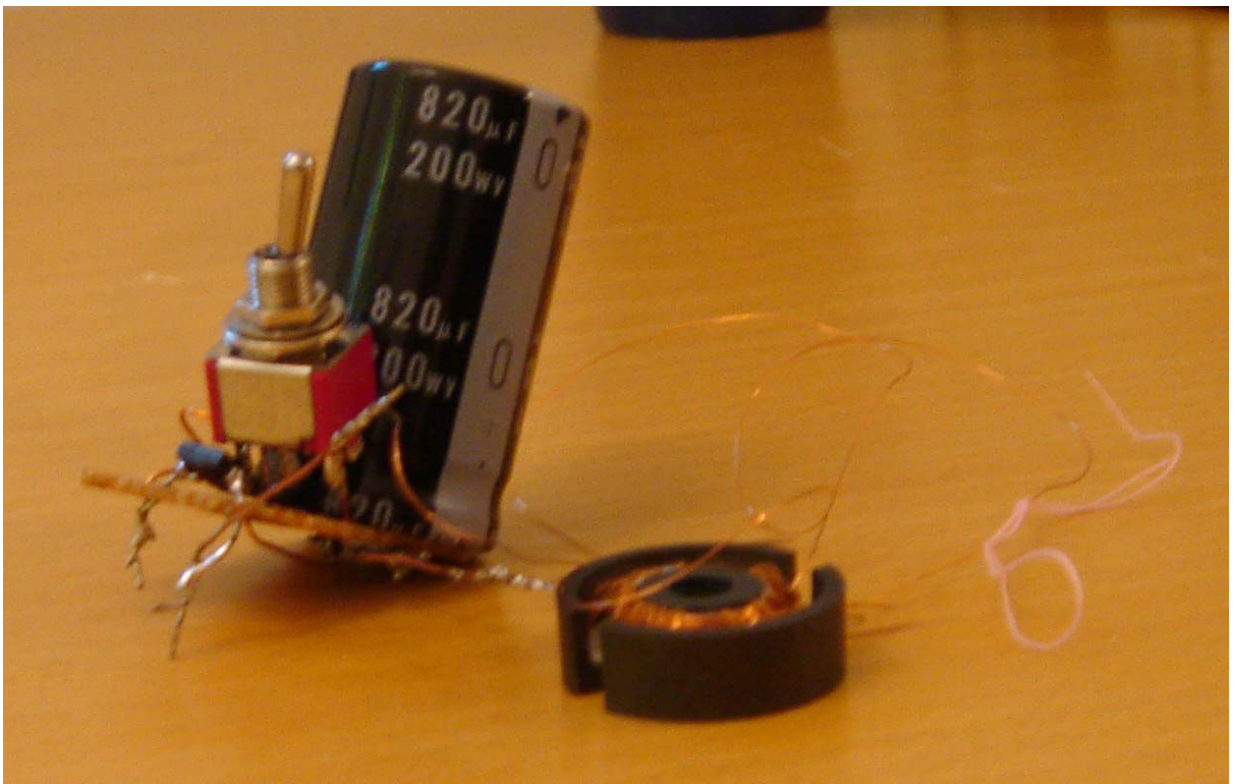
Figure 20: Portable secondary
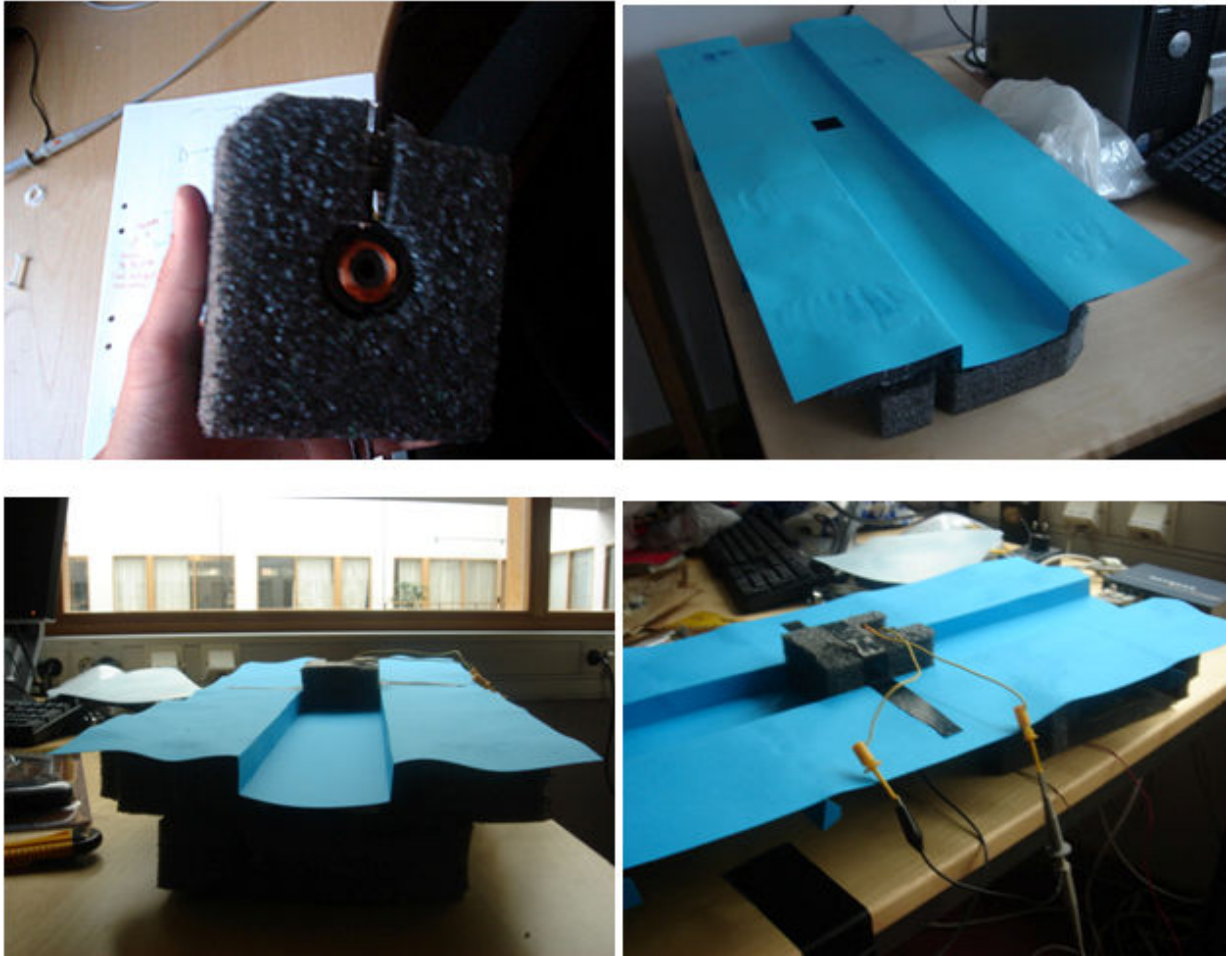
Figure 21: Views of the pad (upper lefthand corner), and Rail (upper righthand corner), and combinations of them (the lower row)

5.4.2. Test #1: Regulated output at the Secondary

The first test took place after winding P&T on one side, and S at the other half of the core, by soldering a bulb between the leads of the transformer at the secondary side. The bulb lit up and the multimiter (although not accurate at all when dealing with high frequency applications) showed a regulated voltage around 16V so the system was performing as the simulations predicted it would. Because the goal of the project requires coupling useful amounts of power a more complicated secondary circuit was needed.

5.4.3. Test #2: τ and effective R identification

The new secondary circuit consisted of a **schottky diode**, to ensure that the current only flows in one direction through the load capacitor. This capacitor is a **470 μF** device, used to

store energy coupled through the magnetic field. Additionally, a **physical switch** was used to control when the capacitor is charging or not. It is also used to discharge the capacitor quickly by shortcircuiting its terminals.
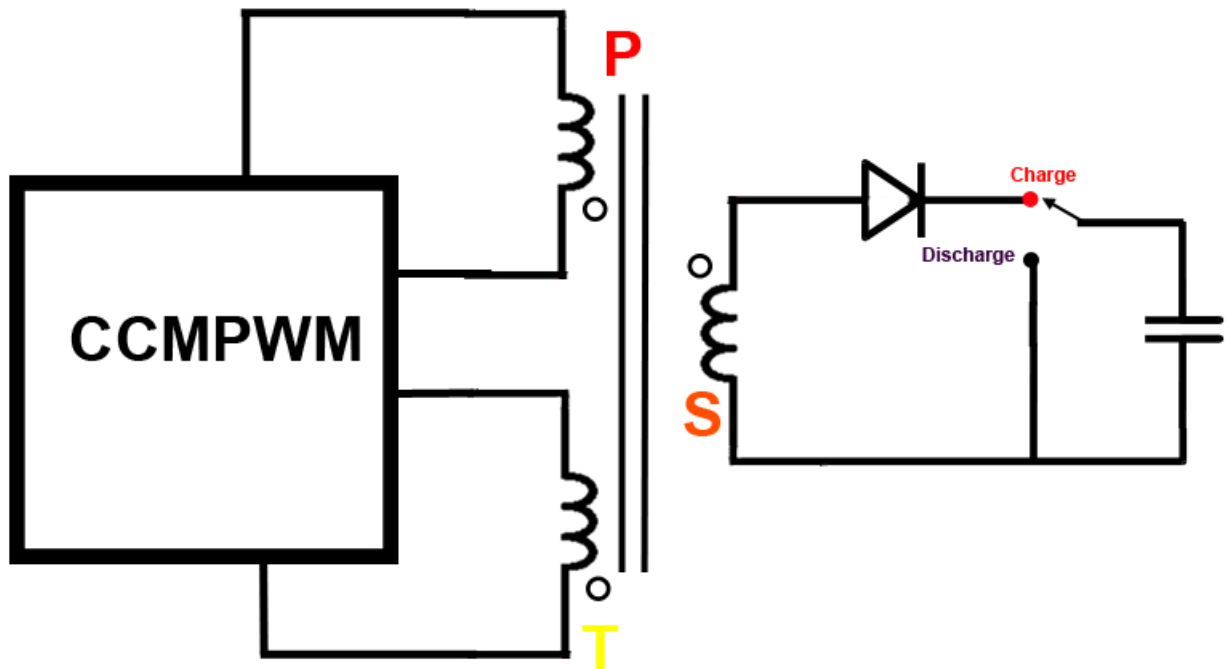
Figure 22: Schematic of the test system for test #2

Initial Hypothesis

Since the tertiary arm is used to mantain voltage regulation and the turns ratio between $N_S/N_P = N_T/N_P = 1$, it was initially thought that the secondary circuit could be modelled as a simple RC circuit because regardless of the controlled ripple, it was thought that the average voltage charging the capacitor would be constant.

Therefore, determining the effective R is important in order to allow us calculate how long it will take to charge a given capacitor before connecting it to the circuit.This equivalent R comes from the internal resistance of the wires constituting the transformer, the diode (in the ON state), and the internal resistance of the capacitor.

Configuration values

The transformer configuration is shown in Table 8, a capacitor of 470 μF was chosen for this test, reaching a final voltage of 8V. Figure 23 **shows the charging of the capacitor due to the secondary coil.**
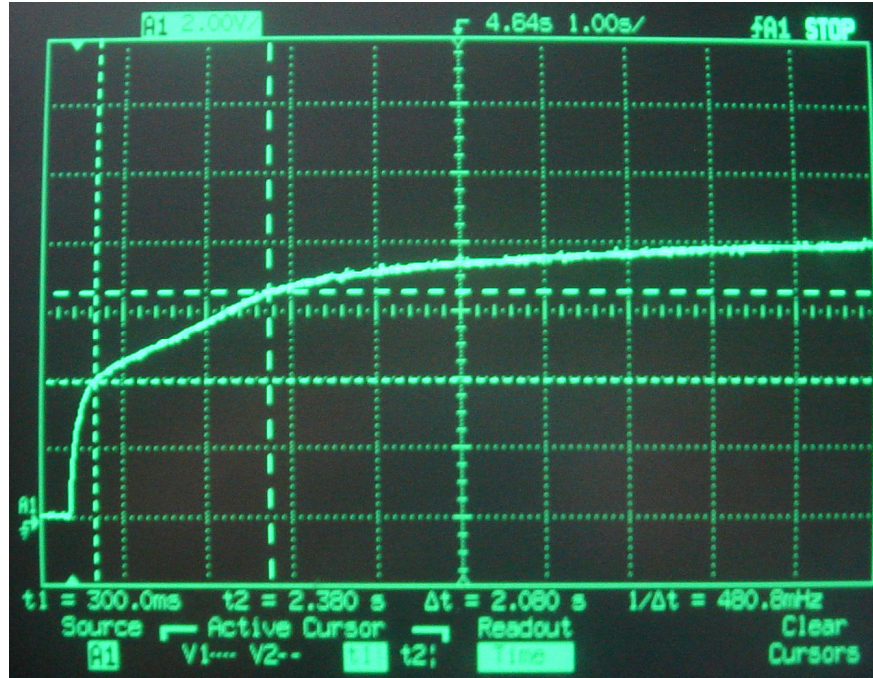
Figure 23: V_C(t) when charging the capacitor connected to the secondary arm

Test #2 discussion: V_C measured at the output capacitor

As shown in Figure 23, the voltage curve doesn't match that expected for a capacitor charging thorugh a fixed resistor. The reason the charging curve of Figure 23 does not resemble an ideal curve (such as shown in Figure 7) is because the source is not an ideal independent DC voltage source. This is because the SMPS is a feed-back system that mantains a constant voltage on the FB pin by changing the electric current set through the transformer primary. This required me to revise my initial hypothesis, because it proved to be wrong. Considering the general expression describing the charging of a capacitor by a DC voltage source:

$$i_C(t) = C \times \frac{dV_C(t)}{dt} \qquad \textbf{(22)}$$

$$V_C(t) = V_F \times (1 - e^{-t/\tau})$$
$$\tau = RC \qquad \textbf{(23)}$$

$$i_C(t) = C \times V_F \times e^{-t/\tau}$$
$$\tau = RC \qquad \textbf{(24)}$$

We see that current through the capacitor is maximum at the beginning, when the capacitor is empty of charge. While the current flow into the capacitor decreases when the capacitor already has charge on it. That causes the SMPS to see(through the transformer) a variable

load at its output. At the beginning, the load behavior is close to a short-circuit ($Z_L \rightarrow 0$) while towards the end, it approaches to an open-circuit ($Z_L \rightarrow \infty$)

Additionaly, the CCMPWM is using the tertiary in order to mantain the voltage, despite the load on the secondary increasing dynamically. The controller is constantly checking the voltage level on the tertiary through the feedback, FB, path. Thus, once the voltage that is targeted is achieved there, the power supply, SMPS, will stop inputing significant energy to the primary coil, because it thinks it is no longer needed. That's why the initial stage is so steep at the beginning (when the secondary is stealing a lot of power from the magnetic field) and slows towards the end (when the capacitor is charged, hence the secondary will steal less energy so more energy will go into the tertiary causing the feedback voltage to indicate that the system is back into regulation).

The reasoning behind the different stages of the curve are that initially, when the buffer is empty, a lot of energy is drawn from the magnetic field taking the tertiary, which is connected to the FB path, out of regulation and causing the controller to turn the switch ON for longer periods of time. Later on, as the capacitor charges, some time after 300ms for this configuration, the tertiary will indicate that the SMPS is back into regulation, so the MOSFET will not turn on so frequently. In other words, after 300ms the effect on the tertiary of opportunistically placing the secondary coil on top of the primary is less, hence a little power from the primary will bring the power supply back into regulation. In all cases the tertiary is controlling the voltage source. Therefore **the buffer capacitor is not being charged by an independent voltage source, as the tertiary controls the power supply.** Hence the nature of that voltage source will result in a **distorted capacitor charging curve** as compared to the charging from a ideal voltage source.

Finally, another useful result from this test is the fact that **the steepest and fastest part of the charge voltage curve appears at the beginning of the charge process,** when the capacitor is empty, the secondary can draw a lot of current and an almost null $Z_{LOAD@SEC}$ is placed in parallel with the usual tertiary load (when the SMPS is regulated but the secondary side is far away).Consequently, the configuration for maximizing the energy transfer to the secondary will be one giving the maximum voltage to a larger capacitor during a very short time period when charging is initiated.

5.4.3. Test #3: Energy transfer comparison with different C_L values

Initial Hypothesis

The previous test results showed that the initial stage of charging is the fastest. In this test we will try to speed up the process and maximize the power transmission by increasing the load capacitance. Two trials were done in order to compare the effect of changing the size of this capacitance. Although the secondary circuit is an RC circuit with varying R, a higher C will increase τ -- because of the law shown in equation 25:

$$Q = Q_F \times (1 - e^{-t/\tau})$$
$$\tau = RC \qquad \textbf{(25)}$$

Configuration Values

For the test #3.1, the capacitor is $C_{\#3.1}$ **= 470µF** and the transformer configuration is shown in Table 8. After this, the capacitor was changed for a bigger one, $C_{\#3.2}$ **= 10.85mF** (470µF in parallel with a measured 10380µF capacitor) and the transformer configuration kept, reaching finally in both cases (test#3.1 and test#3.2) **8V** at the capacitor on the secondary side.

Plot results:
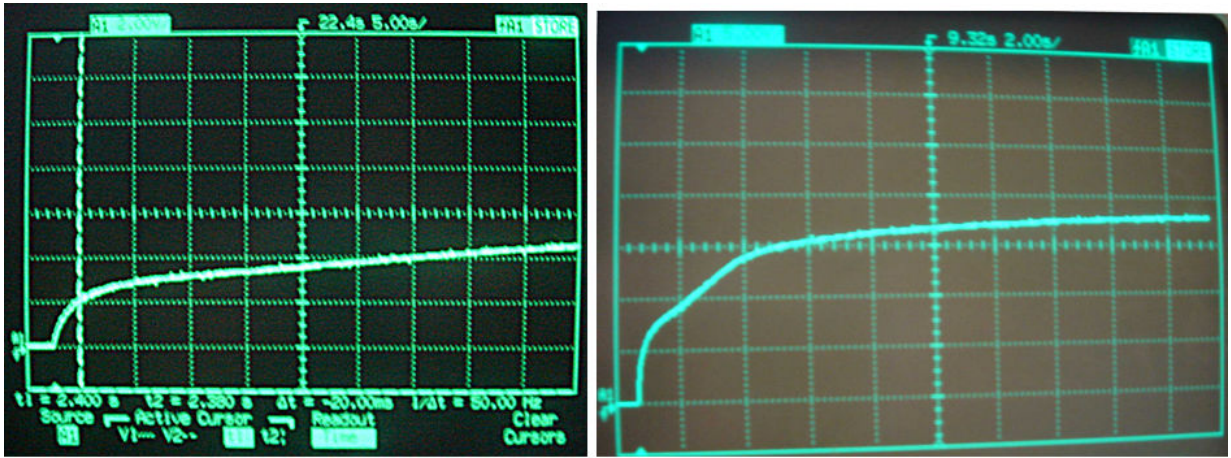
Figure 24: $V_C(t)$ with test#3.1 configuration (left, 5s/div), $V_C(t)$ with test#3.2 configuration (right, 2s/div)

The results are shown in Figure 24. Voltage levels were measured for both configurations at t = 300ms (when the capacitor is still in the first, steepest, and fastest charging stage). Knowing that the energy stored inside an ideal capacitor is given by equation 26 and that power in Watts is the relation between energy in Joules and time in seconds:

$$E_{STORED} = \frac{1}{2}CV^2 = \frac{1}{2}\frac{Q^2}{C} = \frac{1}{2}VQ \qquad \textbf{(26)}$$

Before each test, the capacitor was discharged by means of the switch, to ensure that all the energy stored in the capacitor has been removed before we start transferring any energy via the the magnetic coupling.

Table 9: Test#3 results

Trial	Cap. [mF]	t_0 [ms]	$V(t_0)$ [V]	Stored Energy [mJ]	Effective Power [mW]
#3.1	10.85	300	0,8125	3.58	11.9
#3.2	0.470	300	4	3.88	12.9

Regardless of small deviations due to calculations or measurement errors, highlighted orange values show that **with this turns ratio between primary and secondary** (generating a final voltage in the secondary side of roughly 8V) the **Power transferred is roughly 12 mW** and it's **almost independent of the load capacitance** value. Therefore, the next trial will modify

the secondary output voltage which is the other main variable concerning energy transfer. Note that the amount of energy transferred in 300ms was almost the same in both cases, ~3.7mJ.

5.4.4. Test #4: Energy Transmission comparison with different NS

Initial Hypothesis

Based on the expressions for the stored energy on a capacitor which is proportional to V^2 and on the evolution of the capacitor charge process, where a higher V_{SOURCE} voltage leads to a much higher final voltage at the capacitor, therefore the energy transmission rate can be increased by increasing the turns ratio between N_S/N_P, since the inductance of the coil with the selected pot-core is proportional to N^2. In our case because the core halves are not directly in contact with each other, L will not be exactly proportional to N^2, but it will be close. Thus if the ratio is doubled, then the expected V_{OUT} increase is approximately a factor of four.

Configuration Values

The capacitor here was chosen to be **C = 470µF** and the values for the turns can be checked in Table 10, leading to a final voltage reached at the capacitor at the sceondary of 20V. The resulting plot is shown in Figure 25

Table 10: Test#4 initial configuration

Side	Turns	L_{WHOLE} [µH]	L_{HALF} [µH]
Primary	20	92.7	31.2
Secondary	40	-	150
Tertiary	20	92.7	30
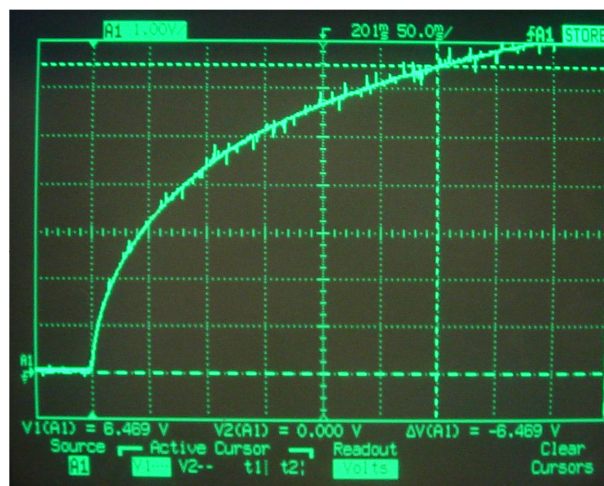
Figure 25: $V_C(t)$ with test#4 configuration

As highlighted in Table 11 with a maximum achieved voltage at the secondary side of the capacitor of **20V** in the same period of time, 300ms, a larger transfer of energy is achieved.

Therefore while the energy transferred increased by 2.54x, the **power transmission is increased** by a factor **2.54** when the 470µF capacitor was used.

Table 11: Test#4 results compared with test#3 results

Trial	Cap. [mF]	t [ms]	V(t) [V]	Stored Energy [mJ]	Effective Power [mW]
#3.1	10.85	300	0,81	3.58	11.9
#3.2	0.470	300	4,06	3.88	12.9
#4	0.470	300	6,47	9.83	32.8

5.4.5. Test #5: Energy Transmission comparison with different N_S/V_{DC}

Initial Hypothesis

The previous test indicated that the energy transferred increased with the number of turns on the secondary N_S. Therefore, different numbers of turns were wound to measure the voltage reached at the secondary, in order to find the optimum configuration for the secondary winding, given a specific capacitor, N_P, and N_T. Tests attempt to confirm or reject the following initial hypothesis: The higher the voltage at V_{IN}, through which the MAX5068 is fed, the greater the energy potentially introduced into the system, thus more energy could be coupled by the secondary to charge the capacitor (faster) and also, the higher N_S (relative to N_P), the higher the voltage induced at the secondary side so, the greater the energy which finally will be stored in the capacitor, see equation (26).

Additionally, in the best case, the transformer should provide ideal power transmission (as seen in section 3.2.) in other words, it will always be true that V_P x $I_P \geq V_S$ x I_S. As a result, a higher V_S leads to greater energy finally stored in the capacitor, see equation (26). The bigger N_S, the longer the wire needed for winding the secondary coil, thus the higher its AC resistance, computed as a result of the variations between ON/OFF every t = 1/f_{SW} which is given by [38]:

$$d = \sqrt{\frac{2\rho}{\omega\mu}} \qquad (27)$$

$$R = \frac{\rho}{d}\left(\frac{L}{\pi(2D-d)}\right) \approx \frac{\rho}{d}\left(\frac{L}{2\pi D}\right) \approx \sqrt{\rho\pi f_{SW}\mu}\left(\frac{L}{2\pi D}\right) \qquad (28)$$

* Where L = length of conductor; D = diameter of conductor, ρ = resistivity of conductor, d = skin depth, $\omega = 2\pi \times f_{SW}$ $\mu = \mu_R$ x μ_O

Additionally, the higher R_{SEC}, the higher the resistance placed in series with a charging capacitor thus, the higher τ and the slower its charging (see equation (23)); however, unless the wire becomes enormously long this effect is unsignificant.

Horizontal misalignment of the cores will reduce the magnetic coupling since fewer magnetic flux lines coming out from the primary will cross the secondary. Additionally the variance of the vertical distance between the cores will modify the equivalent inductance of the **air gap**, thus increasing (until a point) the energy storage ability of the *transformer*: Because the secondary is separable from the tertiary and the primary, there will be a gap between them. This gap is **not a normal gap**, as we are used to seeing in flyback transformers, but it will affect the energy transfer because as the gap gets bigger, the energy transfer is smaller since fewer flux lines will reach the secondary (note that no saturation is happening in this system)
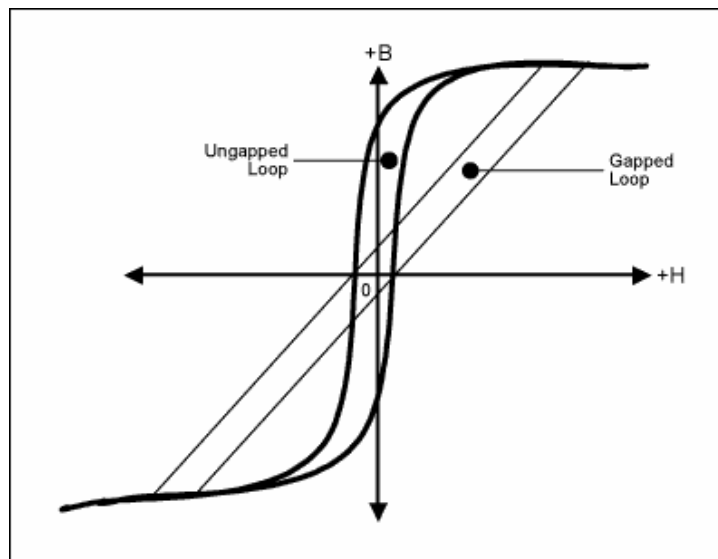
Figure 26: Magnetization loops for a ferrite transformer with and without an air gap. Notice the increase in the energy transfer ΔH when a large air gap is used [40]

The magnetic field absorption capacity of any material is **bounded by its saturation point.** Once achieved, any increase of magnetization won't produce a noticeable change in the magnetic flux density [41]. Therefore, increasing the energy (by increasing V_{DC}) will improve the performance theoretically until **this limit**, when the incremental inductance approaches that of an air core inductor. It seems reasonable that the optimum point should be just before this point, without reaching it. While the MAX5068 has its own requirements (regarding voltages, currents, and inductances) to perform properly, only the secondary will be modified in order to try to find this best operating point, thus only V_{DC} or a closer placement of the secondary side of the core (leading to higher inductance seen by the primary) can saturate it.

A result of working in near field zone with a magnetic field through which energy is being transmitted requires that the separation, is less than 0.16λ, in this case the **attenuation of power $\propto R^{-6}$** which makes the configuration extremely sensitive to really small changes in the relative position between the two cores (either resulting from axial misalignment or vertical separation). However, with our choice of operating frequency of 300kHz, 0.16 of a wavelength is more than 150 m so we are always operating in the near field zone, where this attenuation applies. As can be seen in detail below:

$$f_{SW} = 304878[Hz] \qquad \textbf{(29)}$$

$$\lambda = \frac{c}{f_{SW}} \approx \frac{3 \times 10^8 [m/s]}{304878[Hz]} = 984.000157[m] \qquad \textbf{(30)}$$

$$0.16\lambda = 0.16 \times 984.000157[m] = 157.440025[m] \qquad \textbf{(31)}$$

What this means is that very small increases in the gap will result in large reduction on the power transferred.

Configuration Values

Several experiments showed that the system was very sensitive to small changes in transformer construction. First, winding the coils by hand involves misplacement, imperfections, and small counting errors so a thread was sewn around the windings to fix them into position and an assortment of coils was created in order to use the same coils for all tests to ensure repeatability. This coil assortment is shown in Figure 27.

Second, when installing the coil for each test we must observe correct phasing. Because the secondary *steals* energy from the tertiary when the second side of the SMPS is placed above it, **the secondary and primary coils** must be kept **in phase** to ensure the correct performance of the system. So the end of lead where the winding started around the spool at the secondary, must be soldered to the ground pin of the capacitor, otherwise they will have opposite phase, leading to the tertiary conducting while the secondary doesn't. Therefore the end of lead that had to be soldered to the ground pin of the capcitor was marked with a pink thread, to avoid mistakes.

Figure 27: Coil assortment

Finally, given the influence of the gap between the core halves on the energy transfer by the transformer, this air gap length must be as controlled as well as possible. Three different tests with three different gaps were made by placing between both cores a card (see Figure 30) or 1 (see Figure 31) or 2 (see Figure 32) plastic washers (supplied with the magnetic cores). Similarly, to mantain horizontal alignment and core orientation, a plastic bolt was used to fix both parts, one on top of the other. This plastic bolt was screwed and unscrewed (see Figure 29) by hand for each test. However, it was not possible to maintain exactly the same pressure, so there may be some variance due to the difference in the exact length of the gap.

Table 12: Test#5 separators thickness

Test	Element	Thickness [mm]
#5.1	Card	0.01
#5.2	**1 Washer**	2
#5.3	**2 Washers**	4

In order to handle high voltage levels without damage, a **820μF** capacitor which is rated for 25V was chosen for this test where $V_{DC\ SOURCE}$ took three different values **(12V, 18V, 24V)** as well as N_S went **from 10 to 100 turns** to evaluate the evolution and variation on the behaviour of the system in relation with these parameters. Figures Figure 28 toFigure 32 show the configuration while the results appear on figuresFigure 33 Figure 35 (more information on appendix C.

Table 13: Test#5 initial configuration

Side	Turns	L_{WHOLE} [μH]	L_{HALF} [μH]
Primary	20	92.7	31.2
Tertiary	20	92.7	30
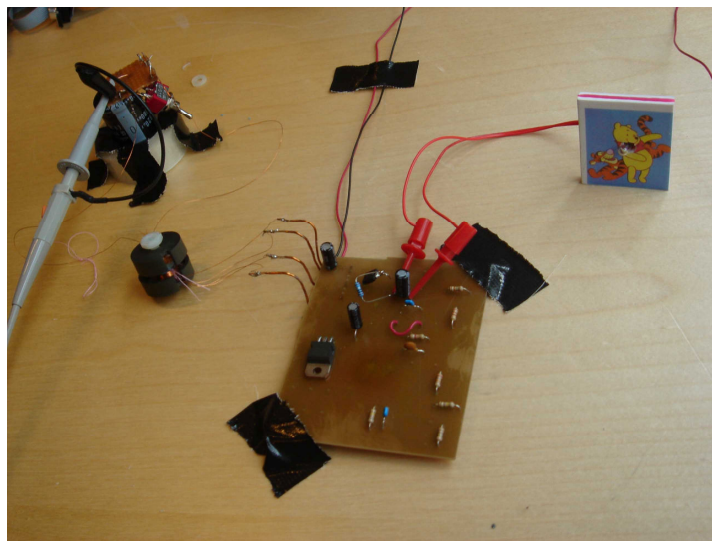
Figure 28: Test#5 configuration
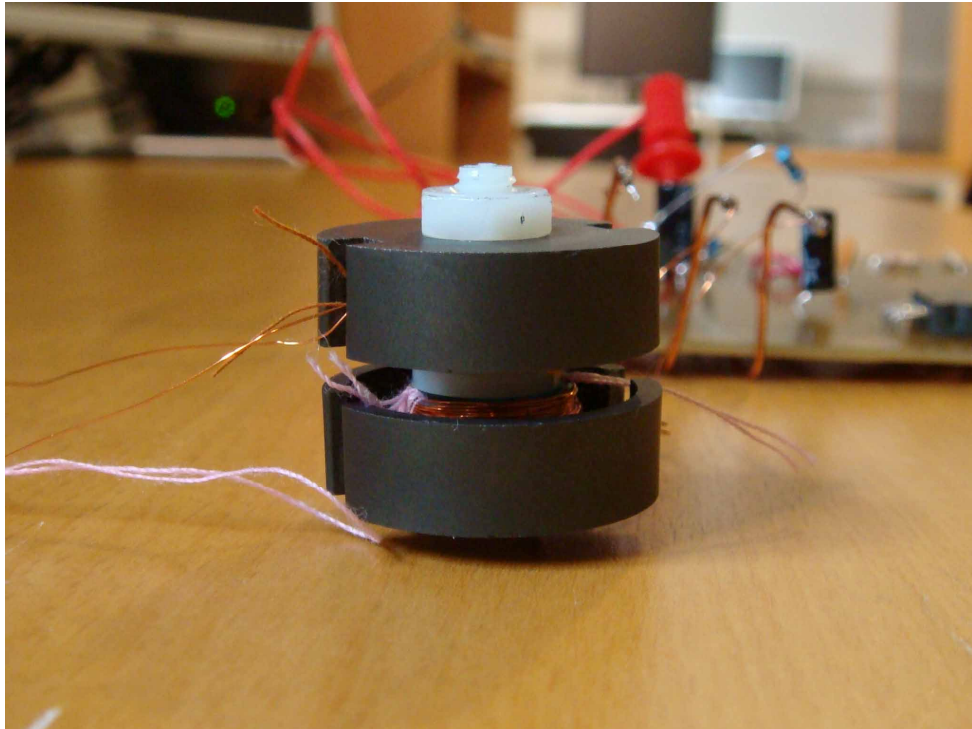
Figure 29: Close view of the stack closed
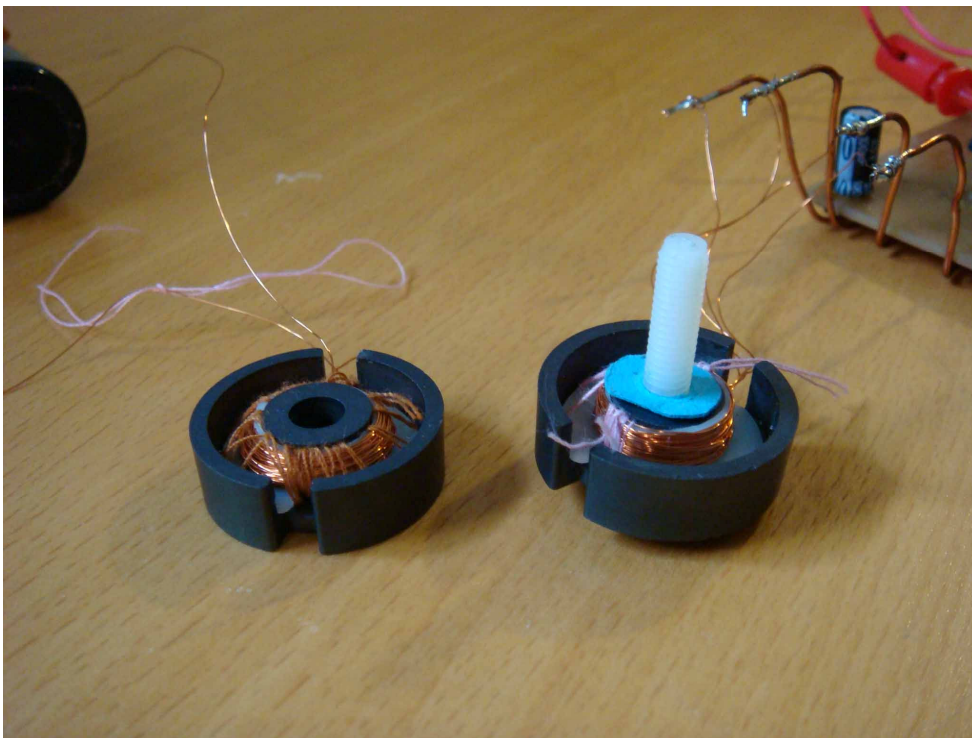
Figure 30: Card between primary and secondary
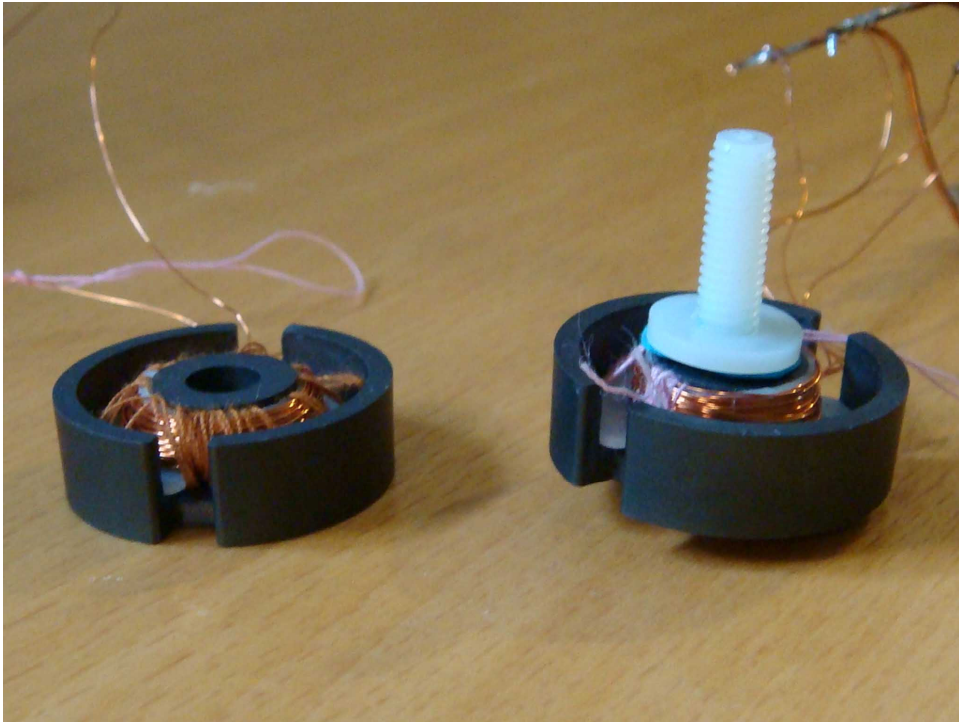
Figure 31: 1 washer between primary and secondary
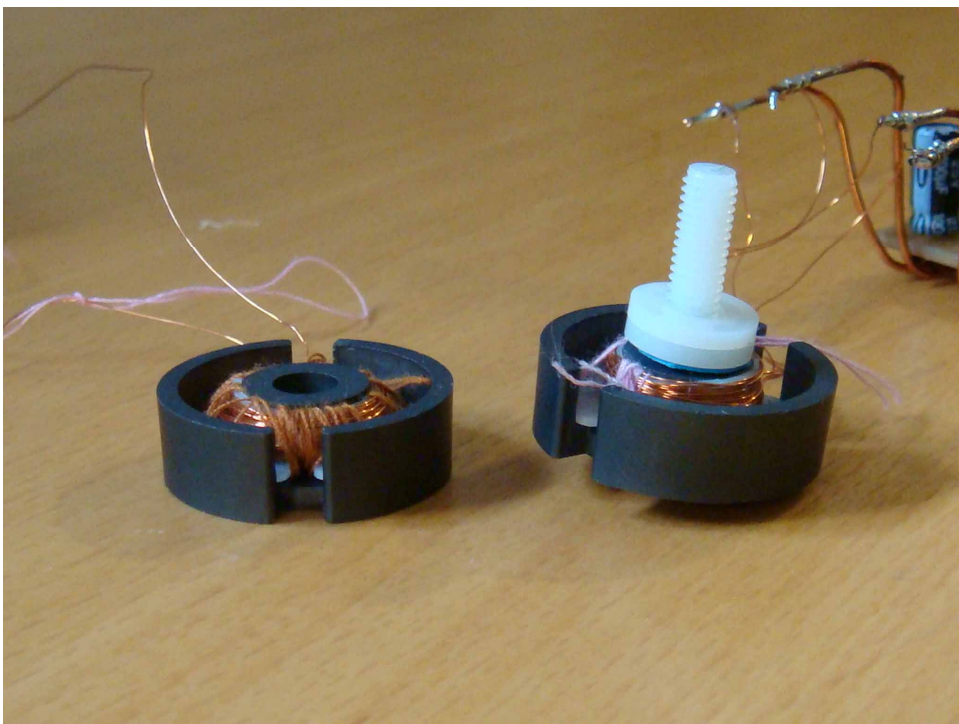
Figure 32: 2 washers betweeen primary and secondary

Data collected

For extra figures and tables see appendix C.
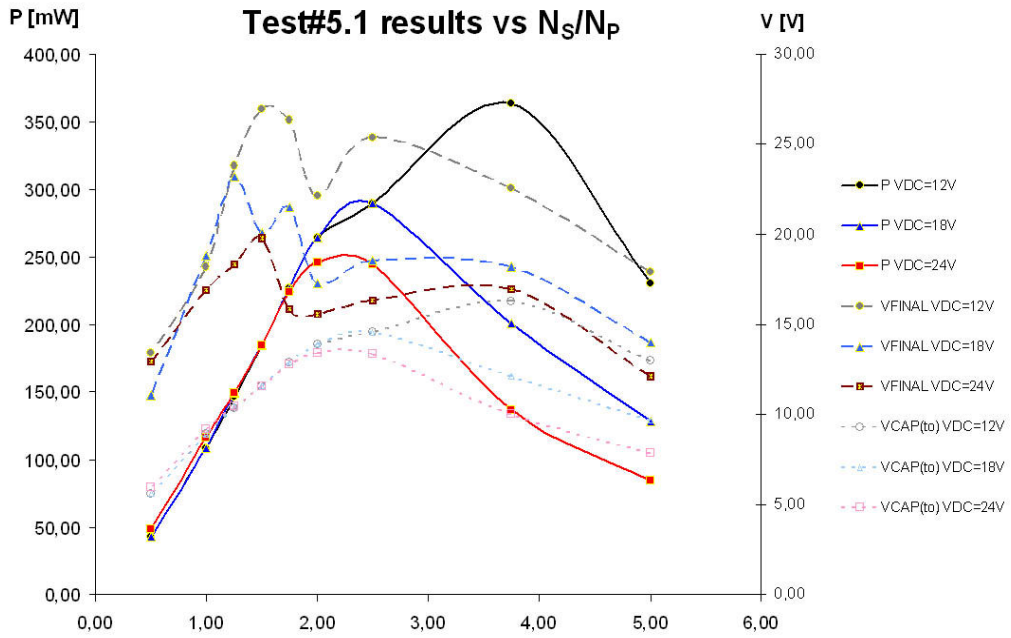
Figure 33: Test#5.1 summary
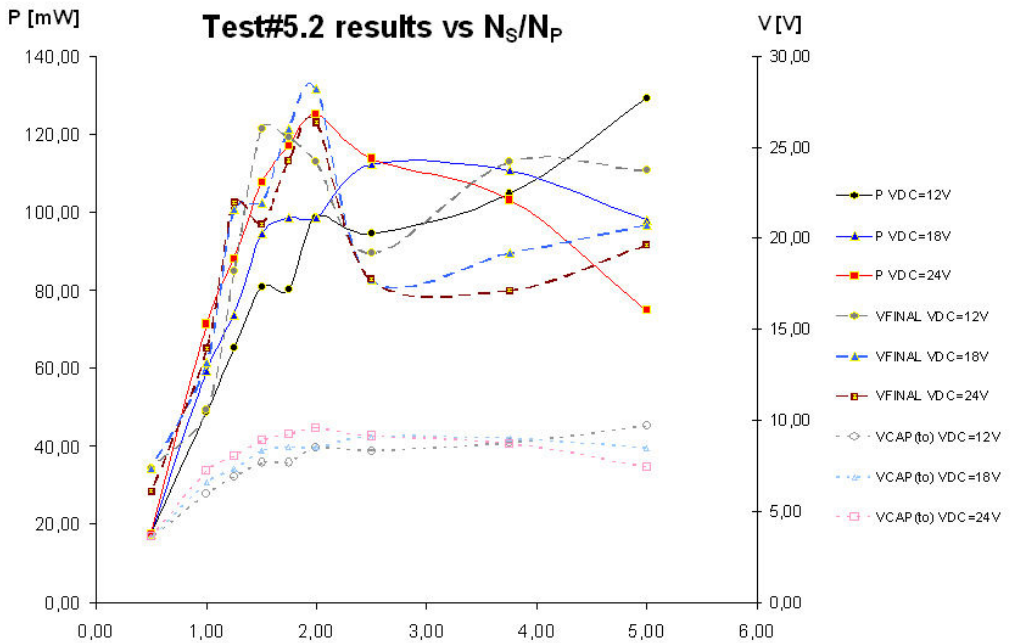
Figure 34: Test #5.2 summary
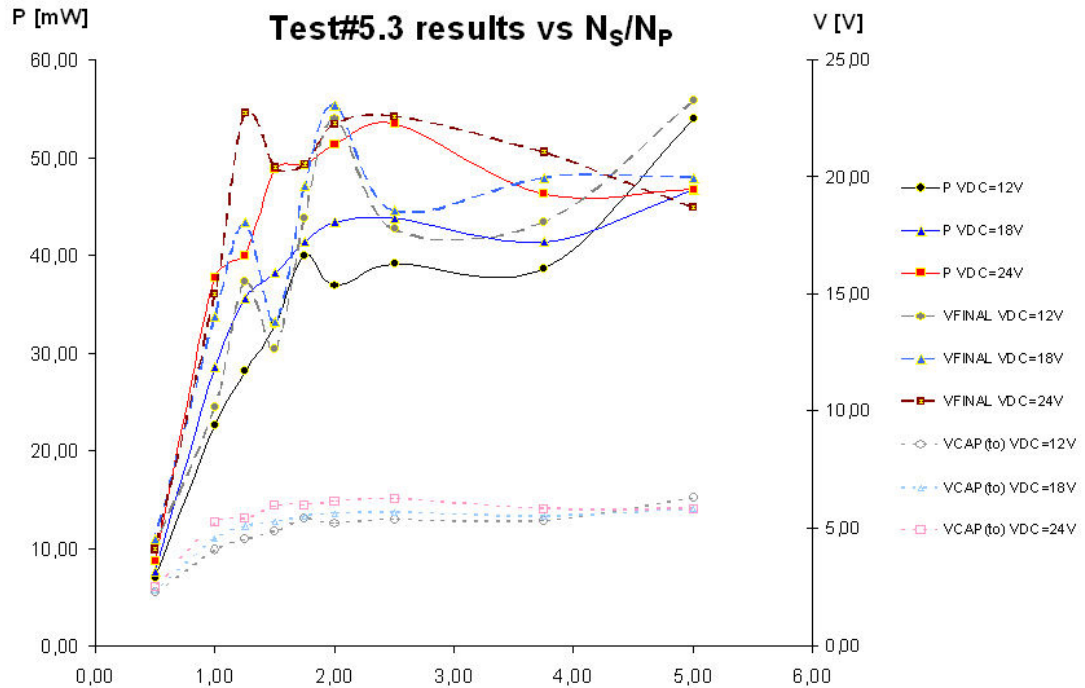
Figure 35: Test#5.3 summary

Power was calculated based upon the voltage reached at the capacitor after t_O **= 300ms** because the estimated time that takes a person to go through the turnstile is around 500ms. This is based upon some simple observations and the empirical value of human walking speed as 2m/s and the turnstile being about 1m long. Knowing power (in Watts) is energy (in Joules) per second, then using equation 26, the power transferred is calculated based upon the energy stored at the capacitor and the time required to transfer it there.

Test#5 Discussion: Comparative graphs and optimums location.

The figures in appendix C, section C.2, compare the behaviour of the system across different input voltage and gap spacing parameters. The data is plotted with respect to either inductance or turns ratio because even if inductance can easily and accurately measured with an RLC meter, the ratio N_S/N_P is actually controlling the relation between the voltages seen at the different ports of the transformer.

Careful inspection of the data from this experiment (shown in Figure 86 to Figure 97) reveals several features. First, for a *real* configuration where the distance will never be less **than that established by the washers (since the devices will always have some sort of cover), shown in figure** Figure 88 **to** Figure 91**, the coupling reaches its maximum** at around **40 turns** in the case of **one washer** or **50 turns** when **two washers** are used. This means that with a **separation around 2-4mm, the optimum voltage is reached with ~50 turns**. The optimum generally shifts to a lower N_S with increasing V_{DC} depite some points being out of the trend such as the result for 100 turns. This can be explained by the volt-seconds law (as previously seen in equation 4 on page 6):

$$L = \frac{V_{ON} \times D}{r \times f \times I_O}$$

A higher V_{ON} achieved through bigger V_{DC} will generate a bigger magnetic flux inside the core, so fewer turns will be needed to balance ohmic losses with magnetic losses. Therefore, the optimum configuration for the best approximation (based upon the configuration with 1 washer) to the real objective is achieved by:

- **1 Washer thus, L_{GAP} = 2mm**
- **N_S = 40 turns**
- **V_{DC} = 24V**

Leads to a **final Power Transmission** of **124,96 mW**.

But, what happens when only the card separates both cores as we can see on figures on section C.2.1 on appendix C? How can we explain the weird trend which occurred when V_{DC} = 12V? Why is the maximum so high and so different from the other data? With the card, the gap is smaller thus the energy storage ability of the transformer is reduced, while closer cores lead also to a higher effective inductance seen at the primary, where the controller is connected. Additionally, by placing the primary and the secondary closer, the number of field lines coming out from the primary and reaching the secondary is increased. Furthermore, the magnetic field lines reaching the secondary are stronger because the distance of the high reluctance path between the cores is shorter in this case (the reluctance of the air gap works against the magnetic field strength like the resistance does against the current).
As a result, the magnetic field between the cores is stronger.

Logical reasoning would lead us to think that this should be the best configuration to maximize the energy transference, but it isn't because if the magnetic field is stronger, the tertiary will have more energy to more quickly bring the feedback pin back into regulation, once that happens we are done, since the charging of the capacitor placed at the secondary will change from exponential to linear evolution as seen in Figure 55 on page 60.

This is a result of the implementation of the system shown in Figure 36. The controller checks the voltage level at the tertiary arm through the embedded feedback path at the beginning of each switching period, which is every T_{SW} = 1/f_{SW}. Only if the V_{FB} sensed is less than what *it should be* as specified by R8 and R9 and explained on section 3.1, will the controller close the switch during that cycle (i.e., provide energy to the primary). When the secondary is far away, regulation is achieved when the voltage V_{FB} is maintained with constant average due to a balance between the energy inputted in the magnetic field by the primary and the energy taken by the tertiary. When the secondary is placed on top, a lot of the energy that was used to maintain V_{FB} is taken by this new path that is demanding a lot of energy to charge the capacitor. Therefore, V_{FB} is reduced from its desired level, forcing the controller to input a lot more energy in the magnetic field. This **energy inputted in the magnetic field** will be used **to charge the buffer capacitor, but also to bring the voltage at the tertiary arm back into regulation.** Thus, the **capacitor** will charge **with exponential evolution until the voltage**

measured by the embedded feedback path is back into regulation, after that, the evolution will no longer be exponential. In short, **once the secondary is on top, the charging time** during which **the capacitor** will charge **exponentially is determined by the time that it takes the tertiary arm to take the FB voltage back into regulation.**
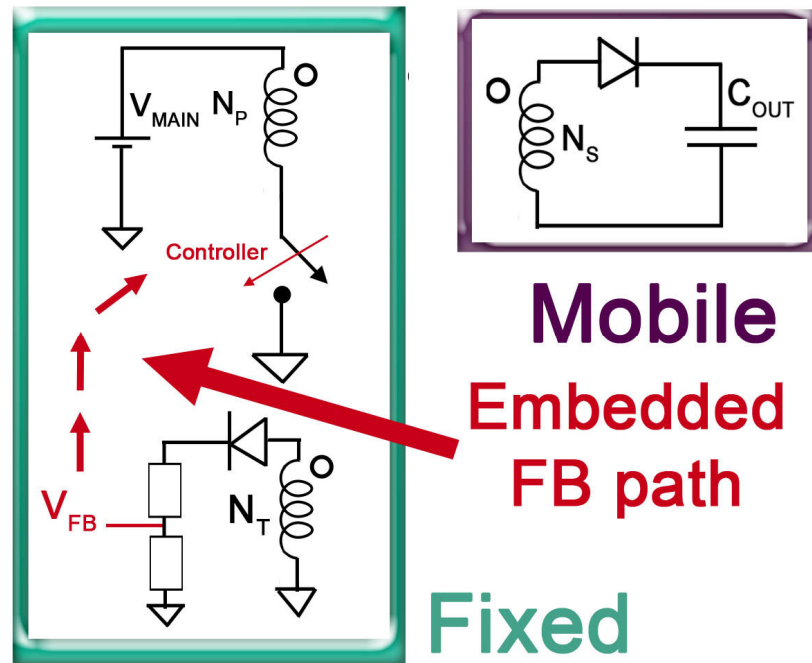
Figure 36: System regulation

Therefore the explanation of the curves with only the card between cores is just that **if the magnetic field is too strong** either because of having the cores very close or resulting from an increase in the energy inputted to the system the FB pin will be quickly taken back into regulation so **the time of exponential charge will be reduced, reducing the energy buffered on it.**

Therefore **a key result** that we have found is that using this circuit **we do not want the controller to return back to regulation once it has detected a secondary over it**, since this will reduce the rate at which it supplies energy to the secondary.

6. Results

6.1. SPICE Model Results

Three different system models with different levels of complexity and abstraction were described and simulated to determine if it was feasible to build such a circuit and specifically to produce a fully-parameterized model where components can be modified and results studied very quickly. As it will be described later, some modifications from the given model were made to improve performance and simplify the circuit, since the simpler the circuit the faster the simulation. It is unnecessary here to go through all the evolutions of the circuit,

from the initial design to the final design so only the primary structure of the code and its final version will be described here. Detailed files and intermediate stages of this evolution can be found in appendix A.

The code is structured with three hierarchical levels of embedded instances in a main file that can be found in appendix B. The code describes the SMPS circuit where the CCMPWM is simply a black-box. The controller as a subcircuit is described in a different file, constituting a second level, this file can also be found in appendix B where the controller is described. This description in turn contains another black-box generating the clock signals, the file can also be found in appendix B. Each of these different parts of the model will be described in the sections below.

6.1.1. sources.cir

The system clock as well as the compensation ramp and the signal used to reset the circuit when the limit of the maximum duty cycle is reached are generated in a separate file to improve legitibility. Therefore the $f_{SW\,of}$ the SMPS is established in this separate file based upon the specified CLK and OSC periods.

6.1.2. CCMPWM.cir
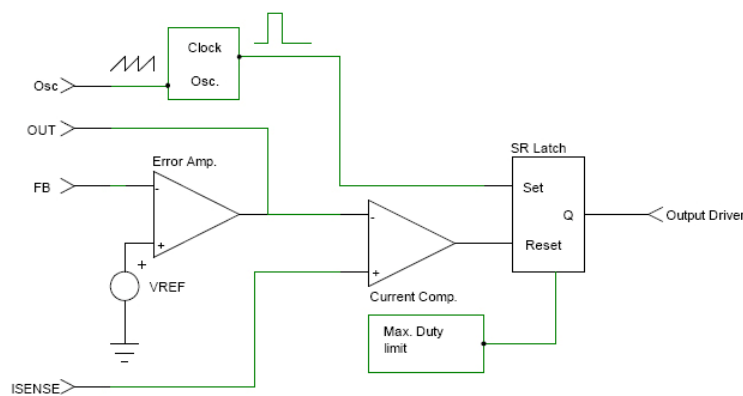
Figure 37: General sketch of the Current Controlled Mode Pulse Width Modulator

The controller subcircuit (see Figure 37), the heart of the SMPS has a really simple behaviour. While the output voltage is sensed and fedback to the controller through the FB pin, the current through the coil is sensed and fedback by I_{SENSE}. If the switch is OFF, then no current will flow across the coil so I_{SENSE} equals 0. First, FB is compared with V_{REF} which equals half the desired output voltage. Initially **FB** was **connected to the output** through a voltage divisor, this was eventually replaced by a **dependent source** in order to achieve convergence, while mantaining the simulation behaviour. If **FB<V_{REF}**, then V_{OUT} still has to be increased, as the load has not reached the desired level yet so **OUT (in the model called OUT_COMP)** will equal **twice the difference** between these two voltages. But, if **FB≥V_{REF}** then V_{OUT}, that it's to say, when the voltage at the load is regulated to the desired level then **OUT** will equal **0**. **OUT** is **compared to I_{SENSE},** which is the addition of the voltage across a resistance placed in series with the coil combined with the compensation ramp signal (a

sawtooth signal used to avoid oscillations). If I_{SENSE}>OUT, then the circuit has to be reset, so the switch turns OFF. While if I_{SENSE}<OUT, then the coil should receive power until the duty cycle limit is reached.
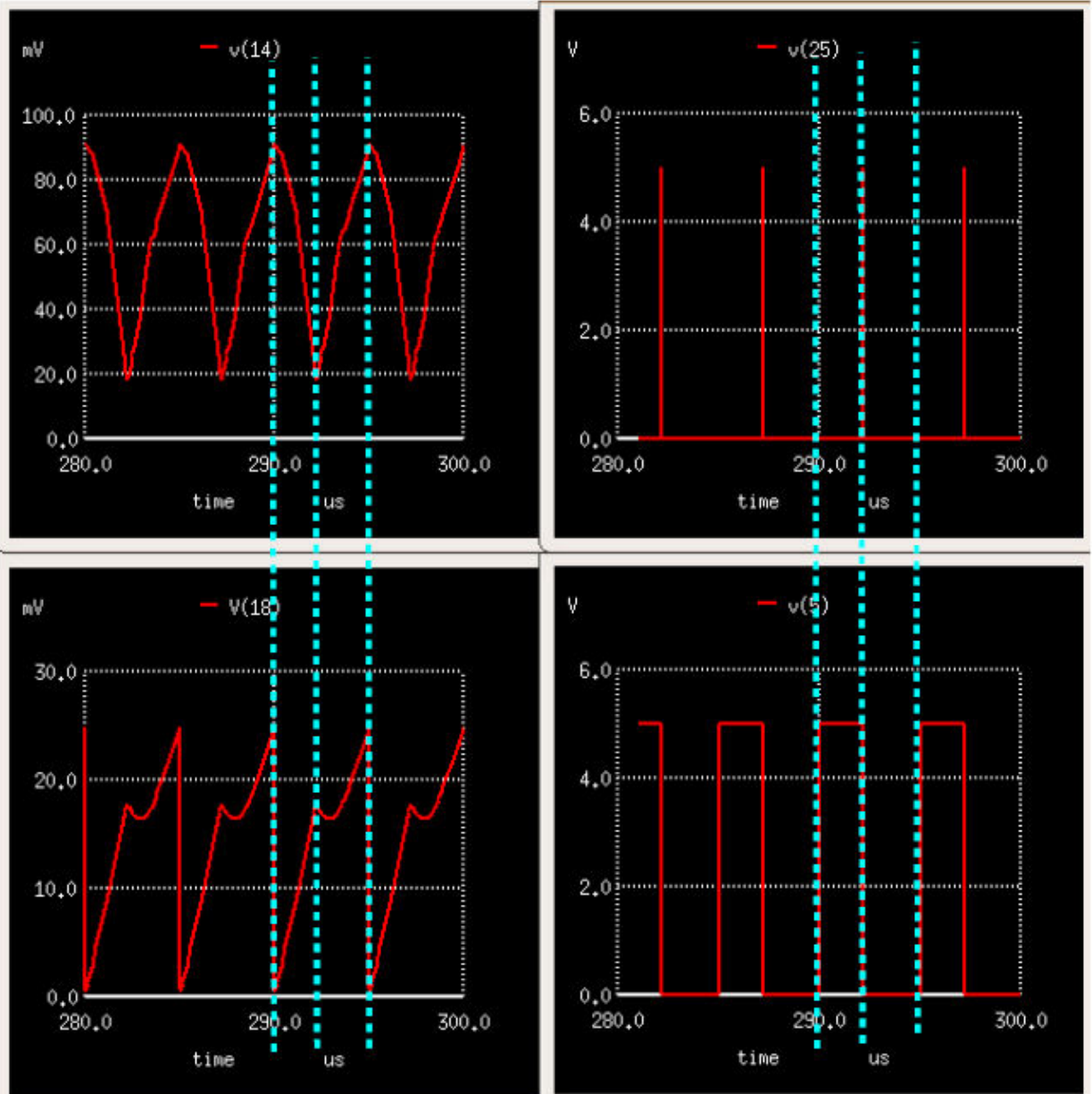
Figure 38:(right, upper and lower): V(25) is OUT_COMP, when it goes up indicating regulated output, that the current is too high, or that the DUTY CYCLE LIMIT has been reached, then, the transistor is switched OFF as indicated in the plot of V(5) corresponding to the MOSFET gate voltage (where HIGH voltage means ON)
Figure 39(left, upper and lower): V(14) is the voltage sensed through the coil while V(18) is the voltage presented to the controller at I_{SENSE} pin, the addition of the (scaled signal V(14)) and the compensation ramp. Using the vertical blue lines one can see that the peak of V(18) is when the MOSFET is turned ON and the signal V(25) turns the MOSFET OFF.

CLK controls the **SET** signal causing the coil to conduct (by turning the switch ON) after every Tclk = $1/f_{SW}$ (= 5us for this simulation) while **duty cycle limit** will **RESET** the circuit (in case the comparison of I_{SENSE} and OUT have not been reset before) after every duty cycle, Duty Cycle = Tclk*D. D = 0.5, this circuit was simulated with a Duty Cycle of 50%, more stable but giving less energy during each ON period.

This system will bring the output voltage to the required value periodically, driven by a **oscilating signal** whose frequency is stablished by CLK. As soon as V_{OUT} reaches the desired value, its average will be a mantained constant, but it will also show a small controlled ripple resulting from the switching between ON/OFF, see Figure 40. These oscillations **make possible the magnetic coupled near fields** through transformer's arms, so **they are fundamental for the system's operation since without this changing voltage, there would be no changing magnetic field and hence no energy transfer.**
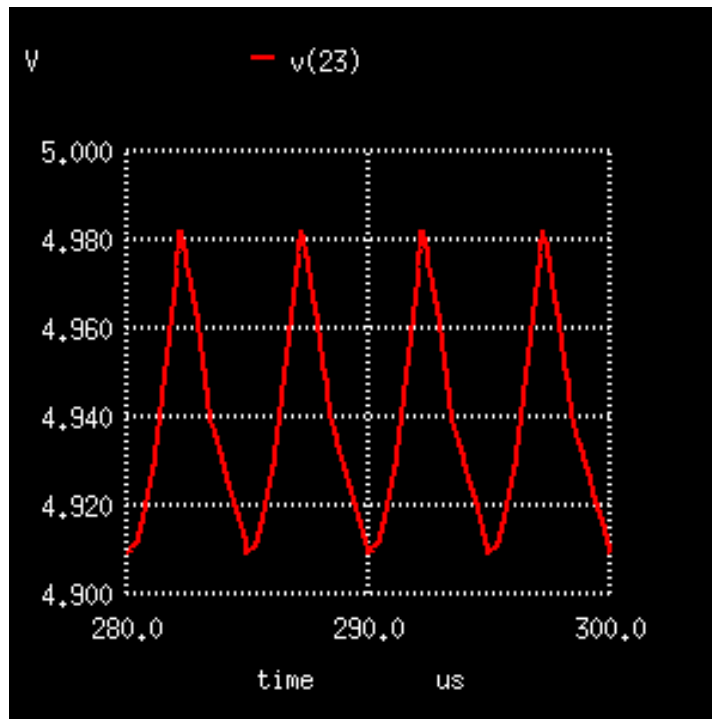
Figure 40: Ripple observed at V_{OUTPUT} when it is regulated to 5V

As shown in the left of Figure 41, at the beginning of the simulation (when the output of the current comparator is zero all the time, because the desired V_{OUT} has not been achieved yet) although OUT_COMP is 0 all the time, the MOSFET switches between ON/OFF periodically. It is turned **ON every** T_{CLK} = 5us = **$1/f_{SW}$,** due to the CLK signal which is triggering SET and **OFF** (in case it was turned ON at the beginning of the period) after **Duty Cycle Limit** (DCL) Time = D*T = 0.5*T in this case which is triggering RESET (by means of a logical OR with OUT_COMP so whenever either OUT_COMP or DCL are activated, the latch is reset). The effect of OUT_COMP is observed in Figure 42 . When the output voltage, V_{OUT}, reaches the desired level, OUT_COMP is activated and the latch is reset so the switch state changes to OFF.
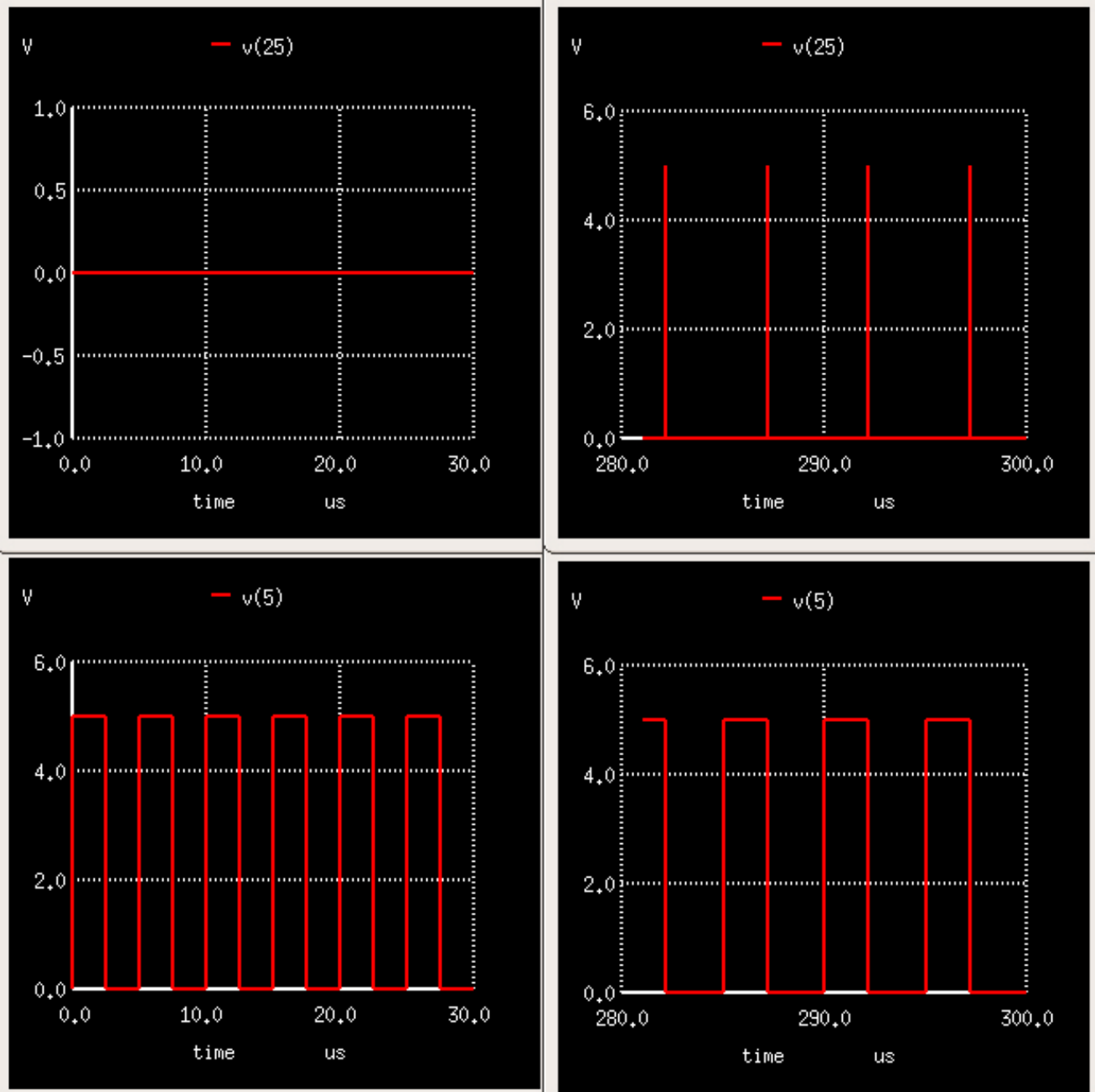
Figure 41(left, upper and lower): OUT_COMP and SET signal at the beginning
Figure 42 (right, upper and lower): OUT_COMP and SET signal with V_{OUT} regulated

6.1.3. Circuit simulation

Having identified the optimum operating point for the system, parmeters were determined to use with a corresponding SPICE file (these files are included as Appendix D) in order to test the reliability and performance of the model. The parameters were chosen so as to simulate something very similar to the real implementation:

Table 14: Modifications to provide a realistic simulation

Parameter	Value	Units
V_{DC}	24	V
f_{SW}	300	KHz
C_{LOAD}	820	µF
R13a = 12V Bulb	200	Ω
C1	47	µF
L_P	31,2 or 92,7	µH
L_S	30	µH
L_T	30 or 92,7	µH
L_{GAP}	2	mm
$\mu_{R\ CORE}$	2000	
$A_{E\ CORE}$	93	mm^2
$V_{E\ CORE}$	3460	mm^3
$L_{E\ CORE}$	37,20	mm
R1 = R_{CS}	0,05	Ω

Xspice's core model [28] requires two arrays relating B with a corresponding H as well as information describing the area and the length of the core. However, a real transformer description can easily be built by entering the data relating B and H to the "*PWL magnetic core model*" combined with three *lcouple* (coupled inductors) instances (one for each transformer's arm) to generate a specific description of the transformer behavior and its influence on the system. To show its function and simplicity, Figure 43 shows how to implement a simple 2-armed transformer with non-linear core.
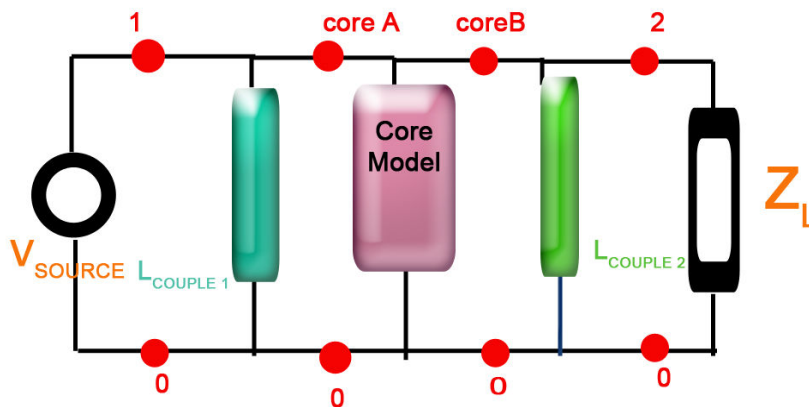
Figure 43: 2-arms transformer with non linear core

Nevertheless the core model shown in Figure 43 was not included because it was not possible to obtain suitable values of B and H to use in the core model leading to faster convergence of the output in the simulation and reducing also the simulation time used to generate results by the simulation environment, ngspice.
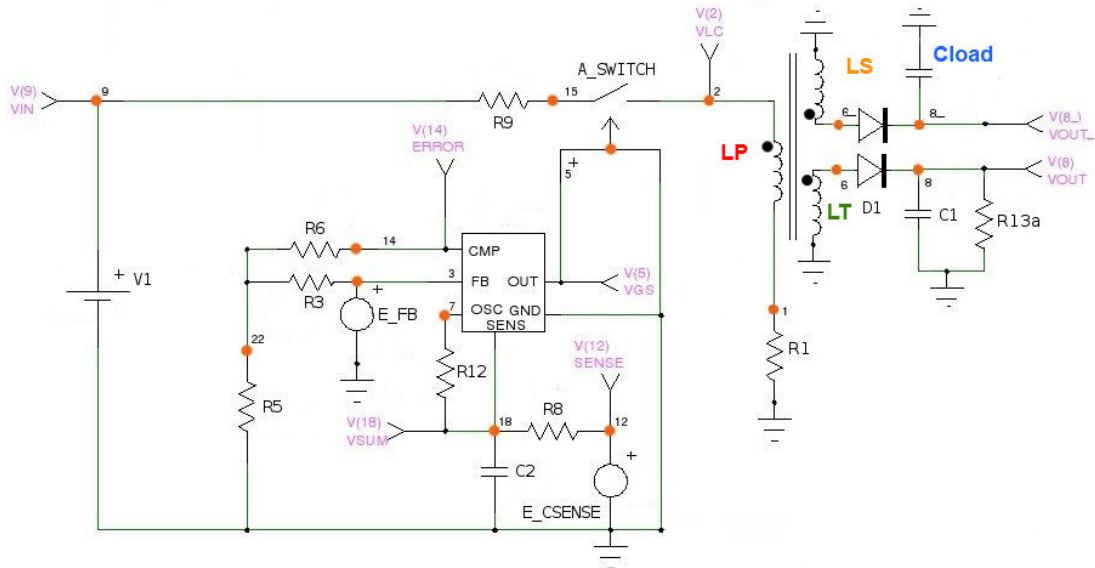
Figure 44: built.cir schematic

The final circuit is shown in Figure 44, where the FB path is shown as a dependent source on VOUT, V(8) so the CCMPWM is still being fooled by using information from the tertiary coil and regulation is maintained without the need for a feedback path linking the handheld device which contains CLOAD to the rest of the circuit.

As the simulation results show in

Figure 45 to Figure 48 the voltage reaches its expected constant level, just as it did in previous versions, without noticing the supercapacitor placed at the secondary side:

- V(8_) is the voltage seen at the capacitor placed on the mobile part of the circuit.
- V(8) is the voltage fed back to the controller, which together with the current sensed through R1, is the basis for regulation.

The figures show the parallel convergence and controlled ripple between the secondary (C_{OUT}, depicted in the figures with the label v(8)) and the tertiary arm, providing FB information (depicted in the figures with the label v(8_)).

They are both regulated to 9V after roughly 150µs with a maintained ripple of 3mV.
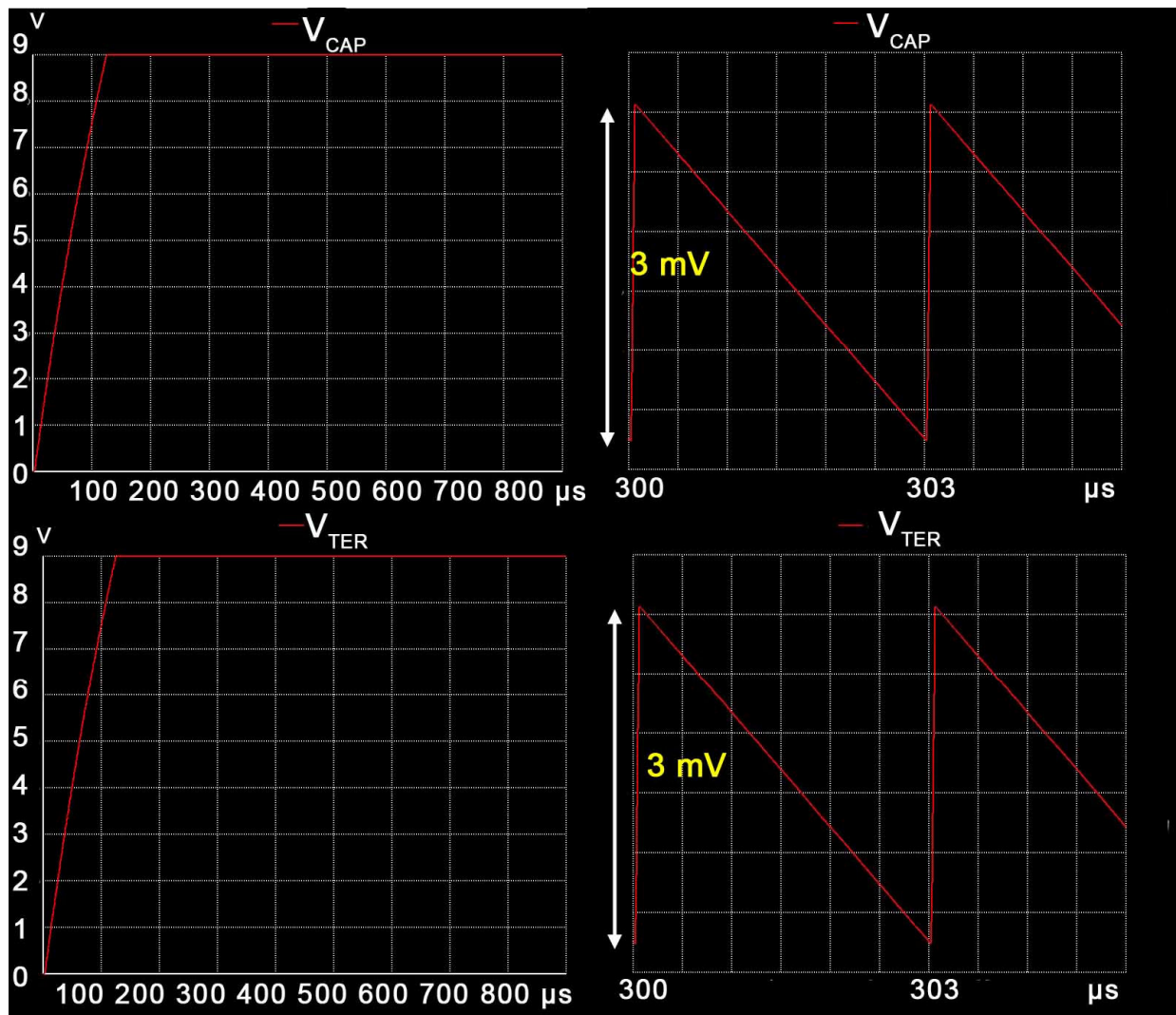
Figure 45(left, upper): Convergence on the output voltage at the secondary (mobile part)
Figure 46(left, lower): Convergence on the voltage at the tertiary arm (embedded FB path)
Figure 47(right, upper): Controlled ripple at the secondary arm, output at the mobile part.
Figure 48(right, lower): Controlled ripple at the tertiary arm

7. Discussion / analysis of results

7.1. Discussion of XSPICE Model

XSpice was chosen because its features supported the circuit which was to be modelled allowing mixed-mode (analog and digital) simultaneous analysis, enabling a real magnetic non-linear functional description based upon a time iterative solution to generate a complete description of the evolution of the circuit's behaviour. The results of this computer model proved it to be a powerful and effective method to predict the behaviour of the system in reality. It was easy to write the necessary SPICE model for the simulation of this circuit.

The convergence at both the secondary and tertiary arms to the voltage level controlled by V_{REF} by means of the magnetic fed back through the tertiary arm was shown to work. In addition, the dependence of the ripple and the convergence time on the components of the circuit, either directly involved on its regulation or influencing it (coils composing the Flyback Transformer, R_{CS} etc.), as well as f_{SW} and the Duty Cycle of the controller were clearly shown. Despite XSpice's advantages, with regard to its fast and realistic approximation of the circuit behaviour, some limitations also appeared. The next paragraphs will examine two of the major limitations.

The larger and the more complicated the circuit, the longer the simulation time if convergence is achieved; however, convergence does not always occur. One must modify many options of the simulation, for example changing maximum number of iterations, time steps, time equation solving methods, and even some features on the model describing the device, in order to find a final solution within a reasonable time. A reasonable time in this case was felt to be less than 1 hour.

A second problem is in the complexity of modelling the transformer. The major problems are modelling the effects of the gap and the effect on the entire structure as the secondary is moved on top of or away from the primary. As a result, building a model that accurately describes the **real** behaviour and interaction of the mobile part of the circuit with the fixed part is really complicated with XSpice. An approximate description which would only describe how things would work with fixed distances between the mobile and fixed parts is easier to implement by means of dependent sources or a user defined model could be written in C once accurate information describing the relation of field intensities and currents on different points of the circuit are available.

In conclusion, the feasible solution is to build an approximation where primary and tertiary are coupled inductor instances sharing the same core, as described in XSPICE with magnetic area, magnetic length and a couple of arrays giving to each value of B its corresponding H. The secondary should be built as the combination of the effects between primary and secondary, but also included the effects of the primary and tertiary. This is a complicated issue currently out of the scope of this Master's Thesis, as the thesis is focused on energy transfer instead of non-linear magnetic SPICE modelling.

7.2. *Discussion of Measurements*

Test#5 combines variations of the parameters that previous tests pointed out to be significant for the system behaviour; such as the ratio of turns and the inductance of the air gap which have important effects on the energy stored in the load capacitor after t_0 = 300ms. Test number five generated the most meaningful results, even though earlier tests also showed the huge impact of the alignment between cores on the energy coupled to the output.

The greater the energy available at the DC source, V_{DC}, the greater the energy that can be coupled at the output. Second N_S, since the higher the ratio N_S/N_P the higher $V_{FINAL\ CAP}$. Finally, L_{GAP} is an important factor to be taken into account because a bigger gap allows a higher magnetic field at the core without saturating it, but it also decreases the intensity of

magnetic field lines because of working in near field, where the power of the field is proportional to R^{-6}. Since we want to maximize the energy transferred to the capacitor the stronger the field in the core, the more energy that should appear at the output. Previous tests showed the extreme sensitivity and variability of the system to these factors, which will each be described below.

7.2.1. Misalignment of the cores

Horizontal nonalignment of the cores (see Figure 49) is an important issue because any small deviation from a perfect overlapping of both core halves has a large effect on the energy transfer due to the decrease in the number of inductive field lines going from the Primary and getting into the Secondary: fewer field lines inside the area defined by the windings generates less current flowing to the capacitor, less current to the capacitor means slower charging and it will lead to oscillations, as shown on the upper part of Figure 50 showing the voltage seen at the secondary side of the transformer (this will also occur when there is poor magnetic coupling).
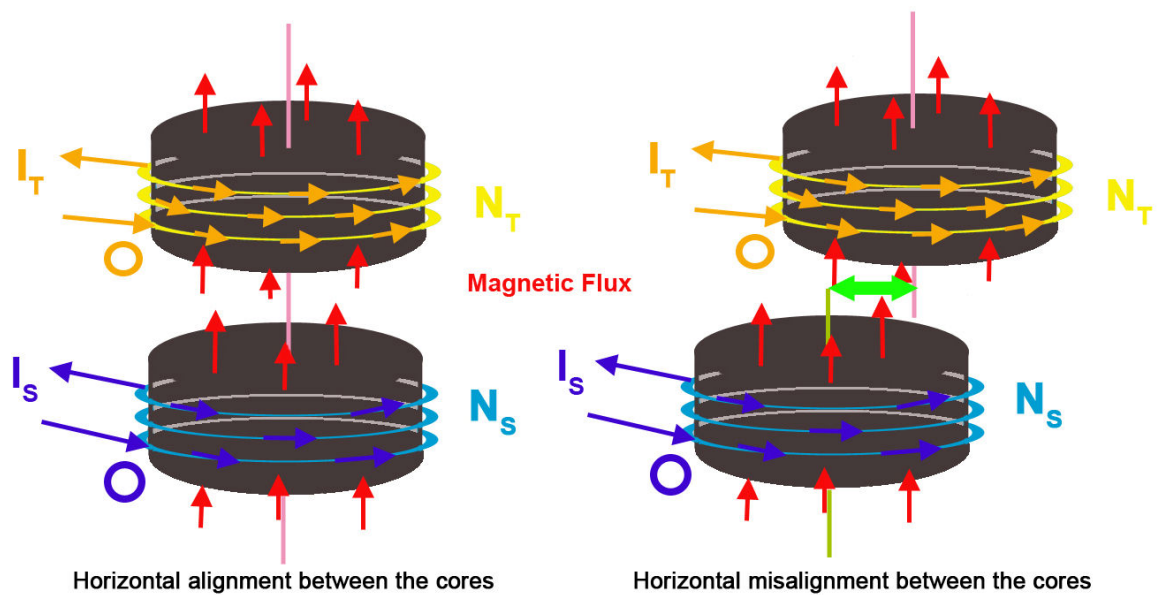
Figure 49: Horizontal alignment
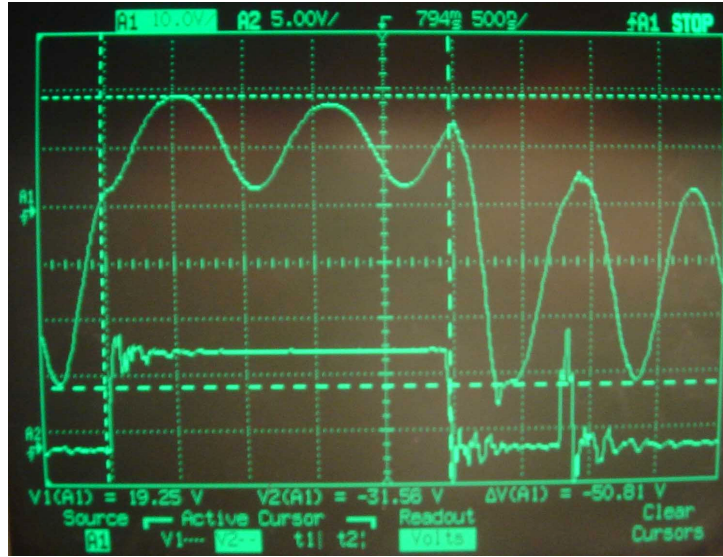
*Figure 50: V$_{SEC\ COIL}$ (upper) vs NDRV (lower) with **faint magnetic coupling***

While with respect to energy coupling **vertical separation of the cores is actually the most important factor of the system.** The system itself is simply a SMPS, in flyback converter configuration. It has been split in two parts by the flyback transformer which is a pair of coupled inductors. The flyback transformer exists in the high frequency stage where energy is chopped as an intermediate step in the DC-to-DC conversion. This is, at the end of the day, the strongest and weakest part of the implementation because on one hand, the tertiary arm will sense when the secondary is placed on top and make the source transfer energy when this happens. On the other, a flyback transformer is a very sensitive device where energy transfer is a direct function of the distance between the cores. The energy is actually transmitted through the small non-magnetic gap in series with the high permeability core material that provides a low reluctance path (reluctance calculations are shown in equations (32) and (33)), in other words, since the reluctance for the magnetic field can be seen as the resistance to the electric current, the bigger the gap is the larger the loss experienced by the magnetic flux between the fixed primary and the secondary, located inside the handheld device.

$$\Re = \frac{\Im}{\Phi} \qquad \textbf{(32)}$$

$$\Re = \frac{\ell}{\mu_0 \mu_R A} \qquad \textbf{(33)}$$

* l[m] length; $\mu_0\mu_R = \mu$; A[m^2] cross-sectional area
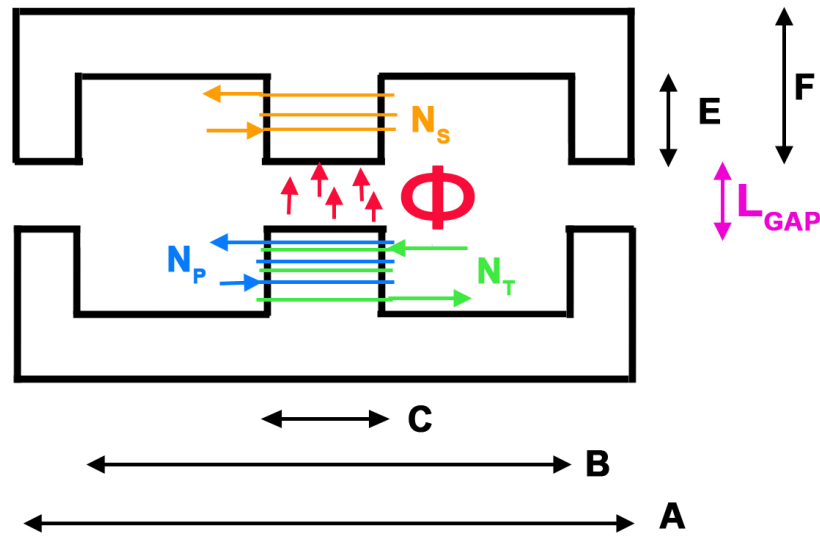
Figure 51: Side core view when secondary placed on top

Nevertheless, our system works in a radically different way with regards to the flyback transformer because here **no energy can be stored at the gap since the secondary is not always on top.** The system is focused on **opportunistic power transference**, this means that **once the secondary is placed on top**, the energy flows from the primary to the secondary core: We want to **maximize** that **transfer by optimizing the trade off (explained in section 6.2.)** between the **time** that takes the source to bring the **tertiary arm back into regulation and the magnetic field strength at the secondary**.

Additionally since the coupling is done through an inductive field working in the Near Field Zone, where **power attenuation $\propto R^{-6}$**, vertical separation will generate a **strong decrease on the field strength**, thus reducing the energy received at the secondary side. Finally, measurements with RLC meter (as well as classic physics) showed that either by changing the L_{GAP} or **placing/removing the secondary** side of the core from the top of the primary **will** also **change** (it will change by a lot, as shown in the charts comparing L_{HALF} with L_{WHOLE}, see section 5.3 and tables 7 and 8) the value of **the effective inductance connected to the primary circuit**. **Consequently, the current there** will vary suddenly, while the controller tries to keep the system regulated (see equation (4) on page 6).

7.2.2. Phase opposition

Phase opposition cannot be forgotten either since the variations of the magnetic field at the core are caused by variations in the current flowing through the wires wound around it and vice versa (see this relation in
Figure 52). So the direction of the field is a function of the direction of the charge flow, as shown by the *Biot-Savart Law [44]* and *Ampère's Law* [45]:

$$dB = K_m \frac{IdI \times \hat{r}}{r^2} \qquad (34)$$

$$K_m = \frac{\mu_0}{4\pi} \qquad (35)$$

Here I is measured in Amperes, dl (unitary vector indicating the current direction), **r** (displacement vector from the current element to the field point), r (distance between current element and field point)

$$\nabla \times \mathbf{H} = \mathbf{J} + \frac{\delta \mathbf{D}}{\delta t} \qquad (36)$$
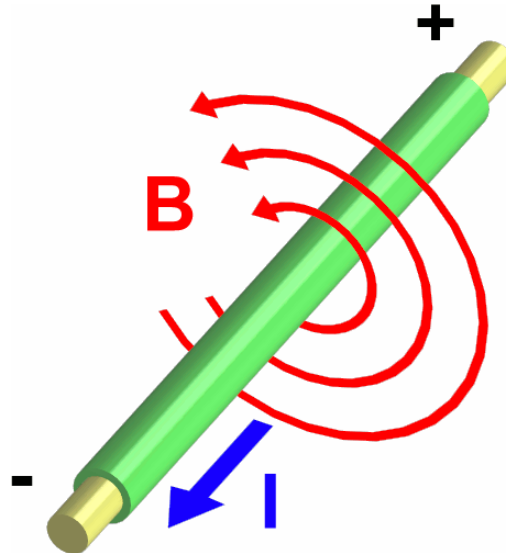
Figure 52: Magnetic field rotating around the wire, direction defined by the current [57]

This means that when the secondary is placed on top, the three sets of windings (primary, secondary, tertiary) will share the same magnetic flux (as shown on Figure 53). Therefore, each coil's terminals need to be connected correctly to ensure the performance and regulation at the SMPS. The terminals marked on the schematic with a *dot* are used to define the polarity need to be connected to an exact point of the circuit. If the windings are overlapped, then those placed first around the core will define the equivalence. Therefore, a wrong connection of this part generating phase opposition between the currents on secondary and tertiary will totally ruin the ability of this circuit where the tertiary tells the controller when the secondary coil is placed on top of the primary by a decrease on the voltage shown at the FB pin. The tertiary, which is wound at the same time as the primary around the fixed core, is in phase with the primary, which means that the diode placed on the FB path conducts when the primary is conducting, but the secondary must be connected to the secondary part of the SMPS taking this phase into account. Otherwise, the secondary will not be able to take any

power from the primary because of this phase opposition, i.e., the secondary will be unable to steal energy from the tertiary. Therefore, if the FB pin is not taken out of regulation, the switch will not turn on for longer periods of time so no extra energy will be provided to the magnetic field generated by the primary. Thus the capacitor will not charge as rapidly as if the secondary was correctly phased with the primary (and tertiary).

When connected incorrectly, the charge takes longer than what it should be because, as shown in Figure 54, the secondary coil will have a positive voltage (causing current to flow through the diode) when the switch is OFF: This SMPS is running with a maximum Duty Cycle of 75%, what means that if conducting on that cycle, 75% of the time the switch will be ON (25% of it, it will be OFF), therefore phase opposition generates **shorter conducting periods on the secondary hence slower capacitor charging and lower power transmission.**
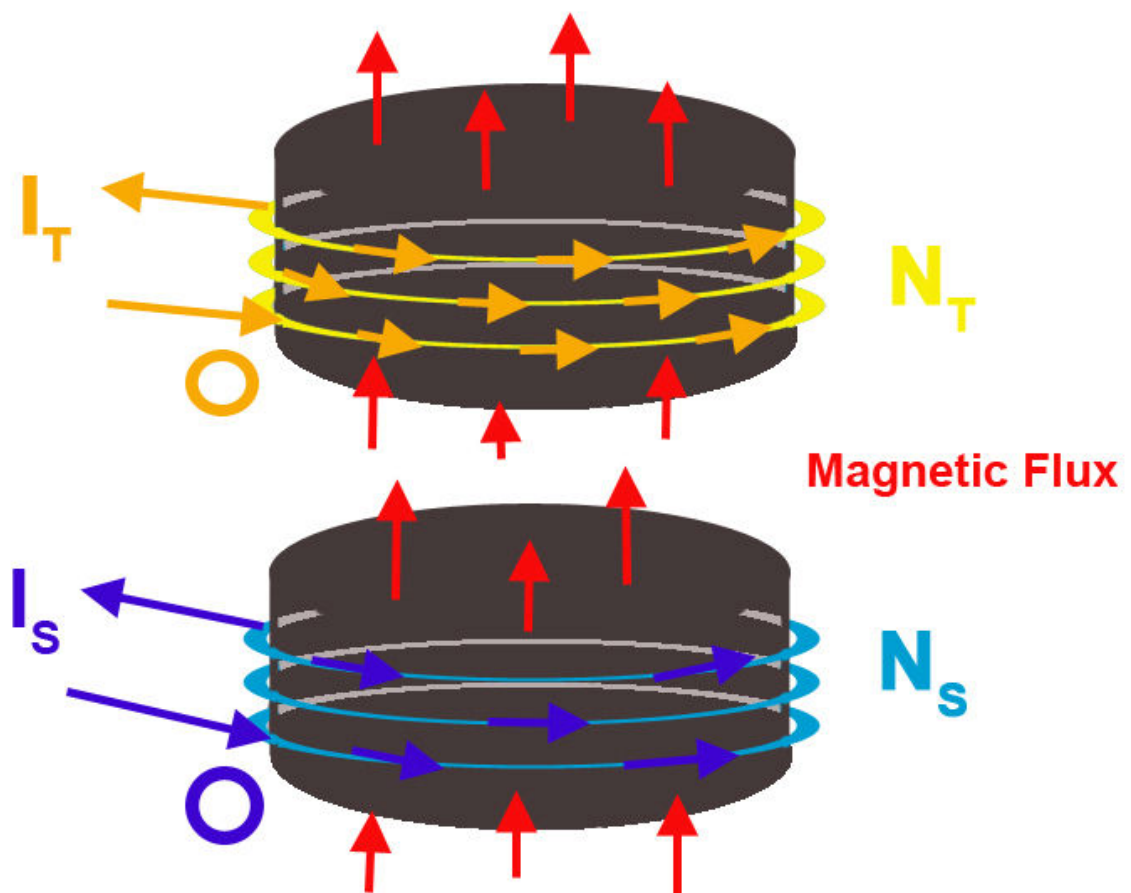
Figure 53: Electrical equivalence between transformer arms
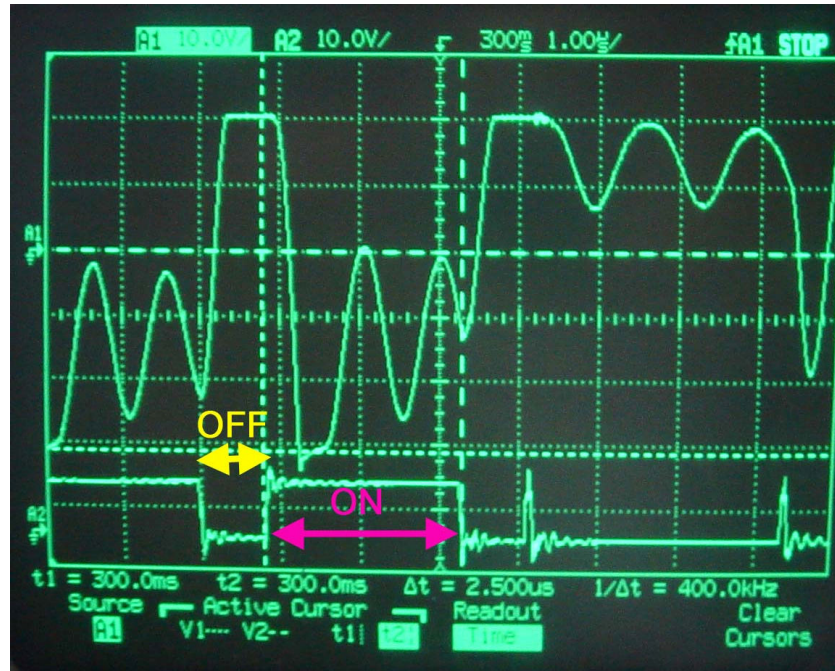
Figure 54: V$_{SEC}$ (upper), NDRV (lower) when secondary soldered wrongly, with phase opposition

7.2.3. Considerations when making measurements

As a result of all the described variability of the system behaviour no matter how carefully one measures. Therefore, the **circuit was removed from the rail** (shown earlier in Figure 21 on page 30) **and the measurements done in a highly controlled configuration** where horizontal misalignment was avoided by means of a plastic screw aligning both cores one on top of the other while vertical separation was controlled by placing different materials with fixed and uniform thicknesses between both cores (card, 1 or 2 washers shown earlier from Figure 30 to Figure 32). Finally, phase opposition was avoided by connecting the secondary coil to the secondary circuit in the proper fashion, ensuring the correct relative orientation between secondary and tertiary.

Although repeatability of measurements was finally achieved, the data collected using the prototype will not predict the exact behaviour of the real implementation as the L$_{GAP}$ will vary considerably with the user, for example a user placing a handheld device on top of the primary-fixed side of the source can vary the distance between cores more than 2mm while walking, which has a strong effect on the magnetic coupling, as the differences in the energy transferred when placing 1 or 2 washers between them is shown in the figures of appendix C.

The most important results extracted from testing the actual circuit are that, as shown in advance by SPICE simulations, **sensing when the secondary** is on top, will **increase the energy put into the magnetic field and regulation of the voltage at the feedback path is** correctly **done simply by observing the** voltage at the load placed at **the tertiary arm**.

Regardless of different configurations, with better or worse power transmission, the capacitor was always taken to a final voltage level with constant average and controlled ripple, without the need for any connection between the secondary and the feedback path, since this information was *effectively transmitted* through the magnetic field.

Additionally there is a common feature among most of the results gathered from the many different configurations. No matter what the final voltage, and thus the amount of energy finally stored on the capacitor, the first charging stage (time period around 300 to 500 ms) is always really steep, hence during this period of time the rate of transfer of energy is high.

7.2.4. Circuit behaviour

Collected results will be described and related to the implementation through the following section. Different configurations led to different charging curves observed at the load capacitor with regards to final voltage level, inflection voltage level and energy stored at t_0 (where t_0 = 300ms and is the period of time chosen to measure the power as energy stored during a period of time). They are roughly similar with respect to the shape of the curve at different stages during the energy transfer process.
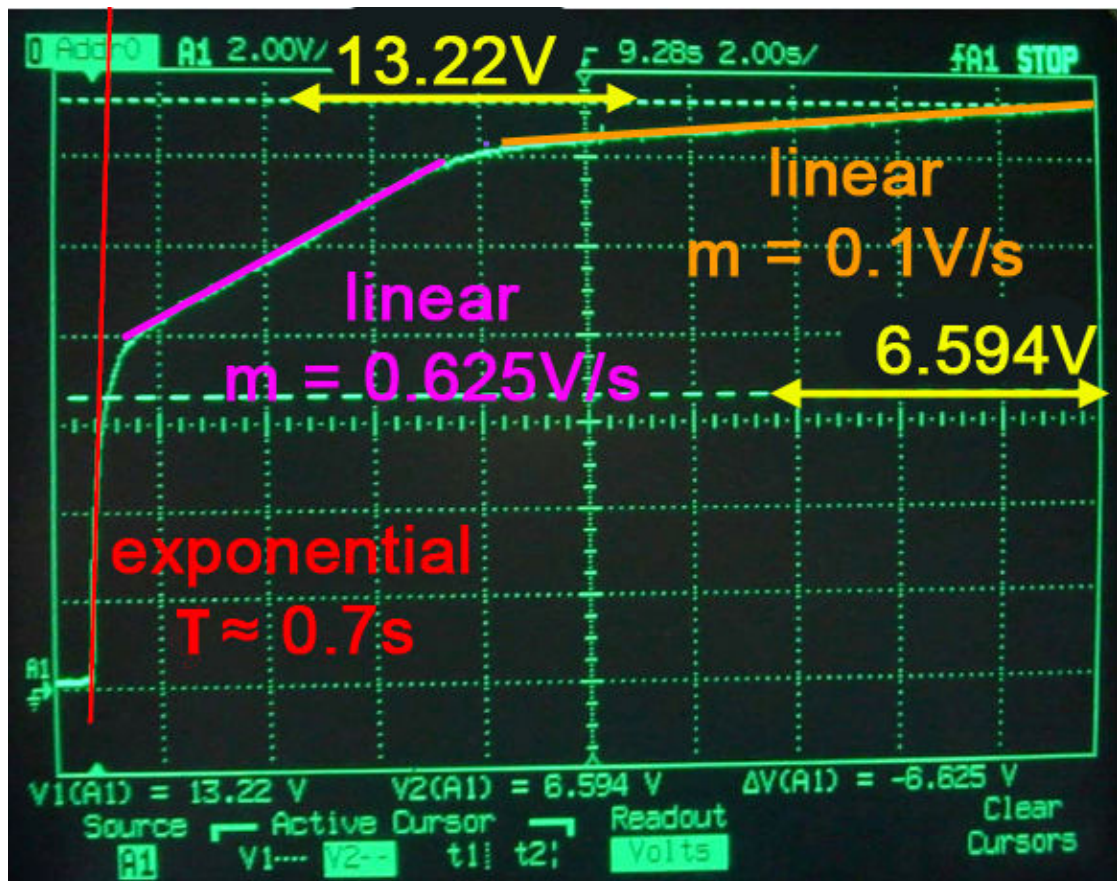
Figure 55: Different stages during the charging process

As shown in Figure 55, the steepest part of the charging process appears at the beginning. When the secondary coil, which is connected to an empty capacitor, is placed on top of the primary winding, a lot of energy is drawn from the magnetic field. This decreases the voltage level at the load on the tertiary taking the system out of regulation and causing the controller to turn the switch ON for longer periods of time. As a result of the large amount of energy that the controller is inputting to the magnetic field, the capacitor will charge with at an approximately exponential rate as described in equation 23, until the voltage sensed through the tertiary arm is back into regulation. Since the three arms share the same magnetic field, the energy provided by the primary is drawn by the secondary to charge the capacitor, but a portion of the field also goes to the tertiary arm, taking the load connected there back into regulation. When regulation is achieved again at the FB pin, the switch will turn ON for only short periods every T_{SW}. Thus, less energy will be input to the magnetic field and the capacitor will charge with linear evolution instead of exponential. Finally, the slope of this linear evolution decreases even more because the more charged the capacitor, the less the current drawn. The resulting decrease in energy transferred means that less energy is stolen from the tertiary - hence even less energy will be made available by the source.

As shown in Figure 55, Figure 57, and Figure 58, different N_S have different V_{FINAL} at the capacitor; but also different inflection voltages resulting from the different voltage conversion rates. Therefore, given a N_S, a change is always observed when reaching the V_{CAP} that corresponds to the regulated V_{FB}., This effect is easily noticeable on configurations with poorer magnetic coupling, either due to smaller N_S or bigger L_{GAP}. While the configurations corresponding to almost no gap seem to have a normal RC curve, even if it's only a result of such fast convergence that it hides this variation (see Figure 56).
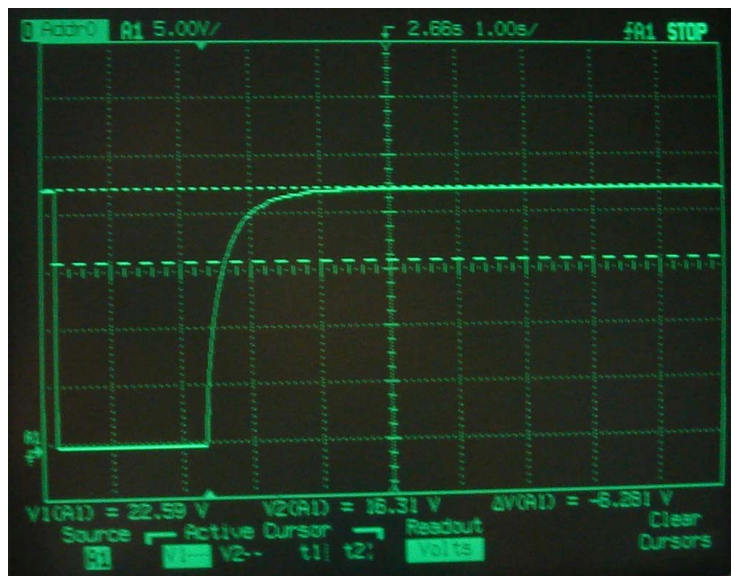
Figure 56: N_S=75, V_{DC}=12V, Card configuration where slope changes are hard to see due to the fast convergence
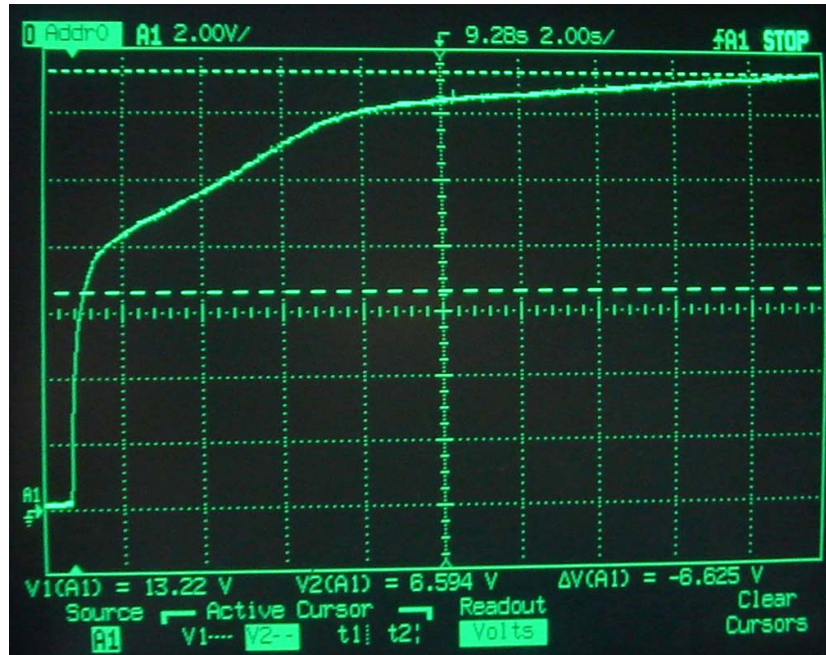
Figure 57: Trend change with N_S = 20 observed around 8V
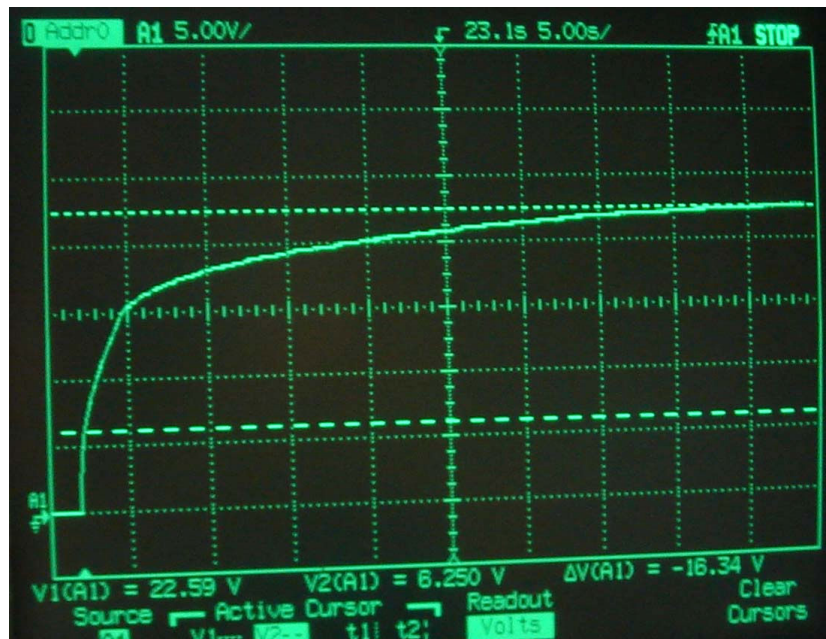
*Figure 58: Trend change with N_S = 50 observed around **17V***

As shown by the comparison in Figure 59, the voltage finally achieved at the load capacitor terminals is determined by the ratio N_S/N_P, but its behaviour is complex because the voltage source that drives the secondary and the tertiary it is not independent but rather completely controlled by the feedback path. When N_S/N_P is small, then V_{CAP}/V_{PRI} vs. N_S/N_P is roughly linear; but when N_S/N_P is larger than 2, then the ratio is either roughly constant or linear but

with a much smaller slope. This would indicate that there are two different phenomena interacting. However, the main phenomenom is the feedback path. It affects the source and controls the amount of energy input to the magnetic field. The source is not independent of the output and therefore the capacitor charging curve will not be purely exponential with a simple RC time constant.
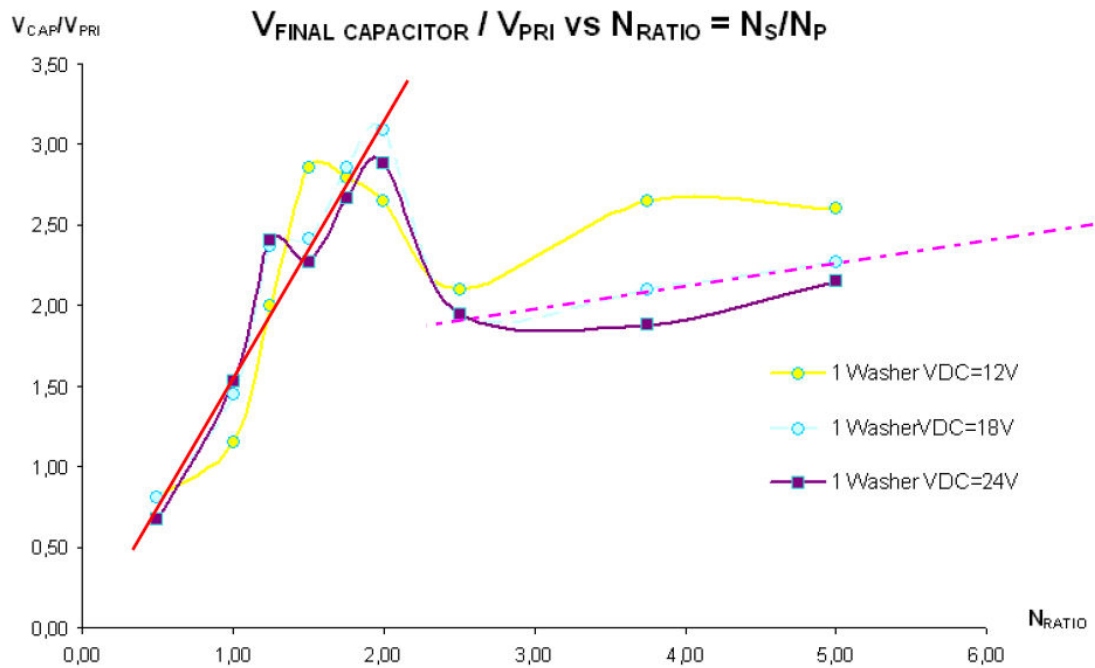
Figure 59: Voltage ratio versus turn ratio

When comparing different energy transferences corresponding to different configuirations regarding V_{DC} and turns ratio, N_S/N_P as shown in Figure 60 for L_{GAP}=2mm, it appears that once the optimum level is achieved, the amount of energy opportunistically transferred during t_0 will be maintained approximately constant. However, it will dramatically decrease when reducing the turns ratio. This is because secondary coils with fewer turns of wire will draw less energy from the magnetic field. This allows the circuit to return to regulation earlier, resulting in the MOSFET turning ON for shorter periods. This distorts the ideally exponential charging behavior.

Recognizing the complexity of the system behavior due to the closed loop nature of the controller and the extreme sensitivity of the magnetic coupling as a function of the spacing and alignment of the core halves, the optimum was searched for and found by trial-and-error. As plotted in Figure 60, the best measured results are those with N_S=40, V_{DC}=24 and L_{GAP}=2mm corresponding to a configuration using 1 spacing washer. The curve using N_S=50 is also close to this optimum.

Power [mW] vs L
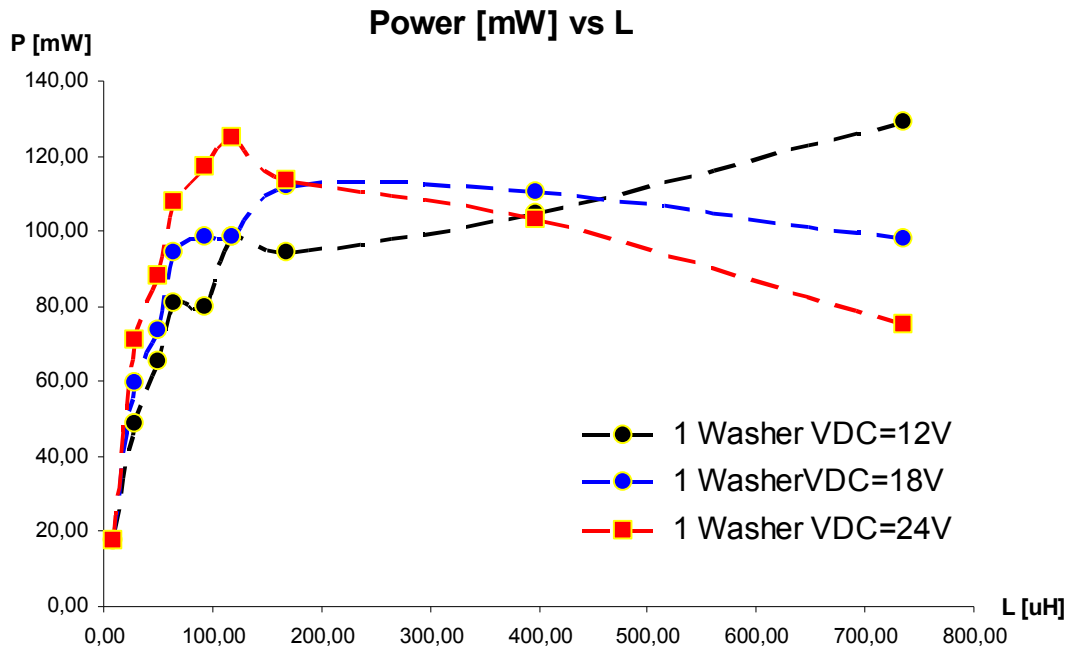
Figure 60: Lower power observed with smallest N_S

8. Conclusions and Future Work

The main outcome of this research are proof the feasibility of energy transfer across a short distance by a near inductive field generated by a small coil wound around a high μ core. This has been shown to be a feasible way of wirelessly transmitting power. This is a significant step forward from existing implementations where energy is transferred with huge coils, rather than concentrated fields (due to the absence of cores in existing designs) [48].

In addition, the implementation that was realized is actually really smart. Power is transferred only when the secondary coil is aligned above the primary coil. Otherwise very little power is consumed, since the load on the tertiary can be quite small. This occurs due to the **virtual feedback path from the secondary, since the tertiary is trying to maintain its regulated voltage. Thus as the secondary steals power from the field, the sensing of the voltage of the tertiary causes the controller to put more power in via the primary**. The power will then be transmitted to the load on the secondary. This **load** is a **capacitor** which **draws a lot of current when empty so it will make the most of the period** while the controller is trying to return the system to regulation. During this time the controller is putting a lot of energy into the transformer's magnetic field.

The current system is an initial prototype. Further optimized circuits allowing higher voltages to be used are possible using the same MAX5068E controller. Future work should explore these circuit optimizations. With respect to safety and electromagnetic interference, it is assumed that no other devices or systems would be affected due to fast attenuation of the

magnetic near field (R^{-6}). However, this assumption should be proven since the MICS band (between 402 and 405MHz) is divided into 10 main channels of 300 kHz [49].

As shown on Table 15, different consumer devices could be powered by this initial prototype for short periods using the energy transferred. Here we consider the optimum power transfer of 124.96 mW in 300 ms as the hypothetical amount of power transferred.

Table 15: Achieved operating time of different low power devices

Device	Battery Capacity [mAh]	Battery Capacity [C]	Consumed Power [W]	Time [h]	Operating Time [s]
Generic MP3		0	0,0192	25	**1,95**
Hearing Aid	105	378		336	**25,09**
iPod NaNo	300	1080		14	0,37
iPod Shuffle	220	792		12	0,43
iPod 5th	400	1440		14	0,27

In Table 15 the time that a device can run was calculated based upon the charge that is stored in an 820µF capacitor during 300ms at a rate of 124.96mW:

$$E_{CHARGED} = \frac{1}{2}\text{C} \times \text{V}^2 = \frac{1}{2}820 \times 10^{-6} \times \text{V}^2 = 37.488 \times 10^{-3} \text{ J} \quad \textbf{(38)}$$

$$V_{CAP\_AT\_t_0} = \sqrt{\frac{37.488 \times 10^{-3} \times 2}{820 \times 10^{-6}}} = 9.562V \quad \textbf{(39)}$$

$$Q_{CHARGED} = C \times V = 820 \times 10^{-6} \times 9.562 = 7.84mC \quad \textbf{(40)}$$

$$t_{OPERATING} = \frac{Q_{CHARGED}}{Q_{TOTAL\_BATTERY}} \times t_{TOTAL\_OPERATING\_TIME\_BATTERY} \quad \textbf{(41)}$$

Or in the case where information about the battery was not available, but the power consumption of the device is known, the calculation simply becomes:

$$E_{CHARGED} = \frac{1}{2}\text{C} \times \text{V}^2 = \frac{1}{2}820 \times 10^{-6} \times \text{V}^2 = 37.488 \times 10^{-3} \text{ J} \quad \textbf{(42)}$$

$$t_{OPERATING} = \frac{E_{CHARGED}}{P_{DEVICE}} \quad \textbf{(43)}$$

Even though the amount of time that the different devices can be run with the energy stored during a 300 ms charge does not seem particularly impressive, it cannot be neglected that this is an academic prototype quasi hand made (i.e. the coils were wound by hand) with almost

all recycled elements from discarded circuit boards and power supplies. In any case, it shows the ability to quickly transfer energy to a load capacitor which could be placed in the hand held device.

So with a cheap system (the cost of the controller is only US2$ while the rest of common elements are much cheaper), energy is transmitted to a buffer which unlike Li-Ion batteries doesn't suffer efficiency problems directly depending on the load connected to it. Energy is waiting within the capacitor's plates to be used. There are many low power devices that could exploit such a system.

Given its fast charge slope and huge energy storage ability, the substitution of the load capacitor by a super capacitor is one of the first and more obvious improvements to implement. Nevertheless, although these devices handle huge currents without problems, high voltages become a critical issue (most of them are rated for 3 or 5 V as maximum) so there is a need for a special circuit, clamping the maximum voltage across the super capacitor once this maximum voltage is reached; however, this will also increase the cost, size, and complexity of the secondary - however, detailed design, measurement, and cost analysis remains for future work.

As well as this substitution, many features of the system can either be optimized (i.e. f_{SW}, Voltages, Duty Cycle, N_{RATIO}, …)or substituted (different current-mode controllers, different shapes and materials to implement the core, different wires the coils are built with) in order to adapt the system to the application one is thinking about. Another improvement is to increase the DC voltage the coil is connected to while keeping V_{IN} directly linked to another DC voltage source. Provided that a N-channel MOSFET can handle voltage levels of 1000V, a lot of energy could be put into the magnetic field. However, additional considerations and analysis to avoid core saturation will need to be performed before this is done.
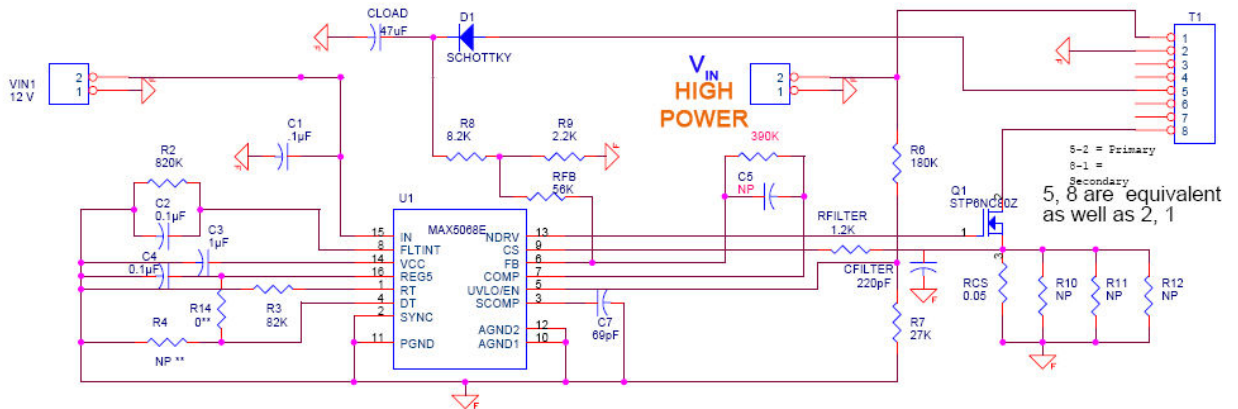
Figure 61: Optimization through higher V_{COIL}

If the charge provided by one primary is not enough (especially as the secondary is rapidly dragged across the top of the turnstile, reducing the time of optimum magnetic coupling) replication and phasing of primaries is a possible solution to provide more energy to the energy buffer. An array of primaries could be built and the secondary sensed (based upon the energy that is stolen from the tertiary) so as to switch each one of the primary coils on as the device moves along. A challenging control problem results from this implementation.

Interferences between adjacent coils won't generate problems since they all share the same orientation.
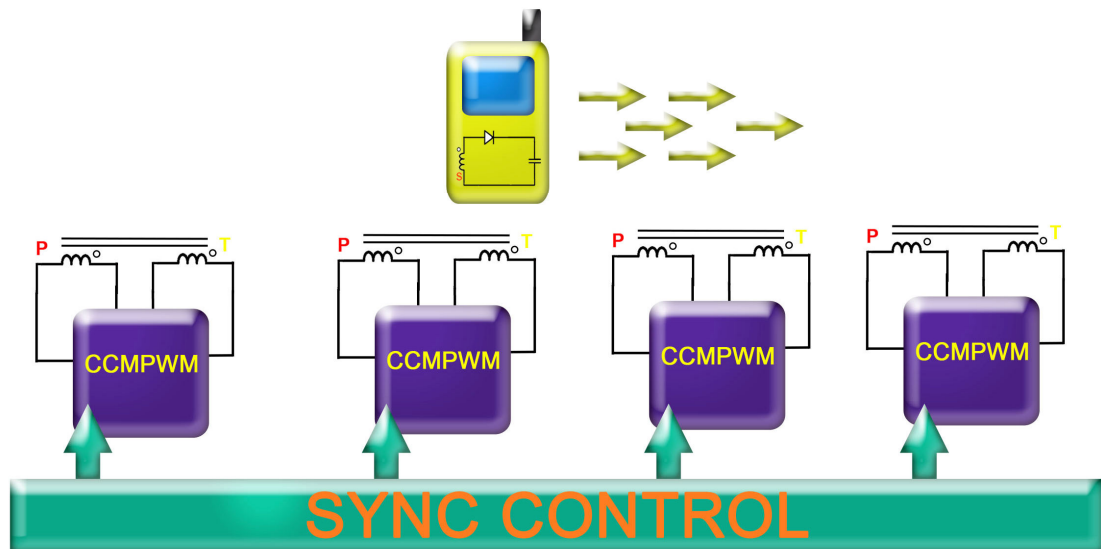
Figure 62: Array of primaries

Another problem is how best to use the buffered energy. Since Li-Ion batteries have very specific and controlled charging requirements, initially it seems that the best idea is to develop an intelligent and efficient way to directly supply the device with the energy buffered on the capacitor. Furthermore, this is directly linked with many research attempts to develop suitable substitutes for current batteries by using capacitors instead [49]. Alternatively, one could make a battery charger, powered by the supercapacitor. So given an array of devices in the turnstile at the entrance of the subway, it might be feasible to power a handheld device, at the same time an RFID tag identifies the user as a *"payer"*.

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Appendix A: Switching Mode Power Supplies

A.1. Introduction

While some concepts about switching mode power supplies (SMPS) seem quite clear, some of these details should be highlighted to explain the reason for the choices made in the thesis. In Switching Power Conversion **Energy** is **drawn** from an "input source", then it's **chopped** into packets by means of a switch (transistor) and **averaged with** the help of an **LC** circuit resulting in something continuous: A **smooth** and steady flow of energy appearing at the output.
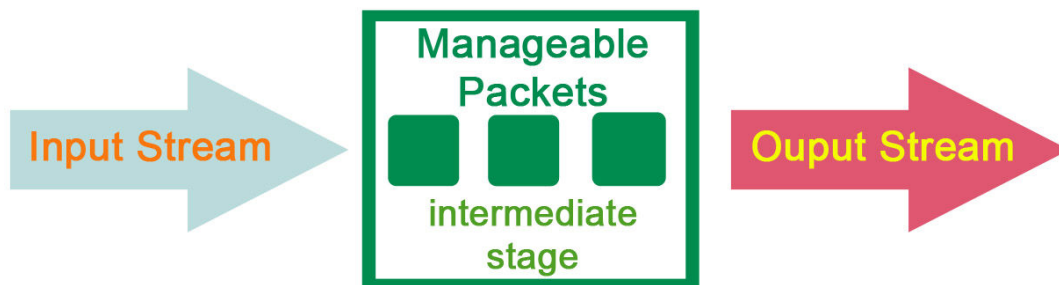
Figure 63: Switching Power Conversion

The higher the frequency at the intermediate stage the better smaller sized energy packets, thus smaller and cheaper components can be used to build the circuit. Additionally, higher efficiency of the magnetic coupling among transformer arms.

Two main kinds of converters can be distinguished:
- DC-DC, transforming a constant V_{IN} into a constant V_O that can also have two main types of regulation either Line Regulation, where V_O is maintained constant while V_{IN} varies or **Load Regulation, where I_O** is maintained **constant while Z_L varies** (it is this form of converter which is interesting for our specific implementation)
- AC-DC, rectification of a varying V_{IN} to generate a constant V_{OUT}

Known the objective of this particular implementation of SMPS is to transfer as much as energy as possible to the output, the choice is a **switching regulator** consisting of coils **L**, and capacitors **C**, since they are reactive elements with energy storage ability that have idealy no loss (even though real devices always have some real power attenuation) so they will minimize losses at the intermediate stage. Additionally, a **diode** is required to avoid reverse currents going through Z_L to keep polarity constant. This is the key for switching between the charge/discharge cycles of reactive elements. A high current **transistor** that will *chop* the energy into small packets at high frequency and **allow the magnetic field to operate** across the transformer arms without saturation.

The objective of this specific design is to couple energy wirelessly (through an inductive field) from the (fixed)primary side of the SMPS, to the secondary at the handheld device, but

transformers require high frequencies, in other words, fast variations on the voltages they see to properly operate:

Faraday's Law

$$\nabla \times \mathbf{E} = -\frac{\delta \mathbf{B}}{\delta t} \qquad \textbf{(37)}$$

In the case of an ideal coil consisting of N turns becomes:

$$emf = -N\frac{\delta \Phi_B}{\delta t} \qquad \textbf{(38)}$$

Where *emf* is the induced electromotive force and $d\Phi/dt$ is the time-rate of change of magnetic flux Φ. The direction of the electromotive force (the negative sign in the above formula) was first given by Lenz's Law.

After this brief introduction to the basis of the technology the discussion about the choice of the most suitable SMPS architecture for this specific goal can continue.

A.2. SMPS main features

In addition to what was said on section 2, **S**witching **M**ode **P**ower **S**upplies are based on the fact that the induced voltage of an inductor always opposes any change in current: When the **converter** reaches its **steady state** this will occur after every switch cycle, thus the average current will be maintained constant. Additionally, *Conservation of Energy Principle* states that voltage levels change through the SMPS while power loss is minimized so as to couple as much energy as possible and *Voltseconds law,* seen in equation 2 [13], indicates that if the **steady state** on voltage conversion is achieved then the **variations on the current through the coil are maintained so the net area under the voltage curve of the inductor is 0.**

$$\Delta I_{ON} = \Delta I_{OFF} = \Delta I \qquad \textbf{(39)}$$

$$V_{ON} \times t_{ON} = V_{OFF} \times t_{OFF} \qquad \textbf{(40)}$$

Consequently a *reset of the circuit*, understood as a return to the same voltage and current the inductor started with is possible at every cycle once regulation is achieved.

So if the Duty Cycle is defined as the relation between the time the switch is conducting and the whole switching period

$$D = \frac{t_{ON}}{T_{SW}} = \frac{V_{OFF}}{\left(V_{ON} + V_{OFF}\right)} \qquad \textbf{(41)}$$

Where $V_{ON/OFF}$ changes in different topologies, while T_{SW} can differ from $t_{ON}+t_{OFF}$

We can define the Ripple Ratio, r, describing variations on the current flowing through the coil as:

$$r = \frac{\Delta I}{I_L} = 2\left(\frac{I_{AC}}{I_{DC}}\right) \qquad \textbf{(42)}$$

During *steady state* in power conversion:

$$L \times I_L = \frac{V_{ON} \times D}{r \times f} = \frac{V_{ON} \times D}{f} \times \frac{1}{r} = \frac{E \times t}{r} \qquad \textbf{(2)}$$

There are three main options among different topologies, leading to three main configurations: **Buck**, a step-down converter, in other words, $V_O < V_{IN}$. While the **Boost** does step-up conversion leading to $V_O > V_{IN}$. Finally, the **Buck-Boost** can either be step-up or step-down, consequently $V_O < V_{IN}$ or $V_O > V_{IN}$.

A.2.1. Buck Topology

In the basic Buck topology, the inductor is connected to the **output**, so it is characterized by having $V_O < V_{IN}$ and maintaining the polarity constant, in other words, if V_{IN} is greater than zero, then V_{OUT} will also be greater than zero.

In this converter, when the switch is ON, energy from DC source to the inductor and to the load, Z_L, and current goes through the switch (see figure 65) but when the switch is OFF, energy from the inductor goes to Z_L while current flows through the diode (see figure 66). The current flow through the capacitor placed at the output is *choppy* (pulsating) when going in but s*mooth* when going out, but with a null average because the same amount of current goes in/out on each cycle.

As depicted in Figure 67, if $\overline{I}_L$ is the average current flowing through the inductor, then the average diode current which only conducts when the switch is OFF, is defined by equation 44 while the average switch current which only conducts when the switch is ON is given by equation 45. Therefore the relations described in equations 46 and 47 are true.

$$\overline{I}_{DIODE} = \overline{I}_L \times (1 - D) \qquad \textbf{(43)}$$

$$\overline{I}_{SWITCH} = \overline{I}_L \times D \qquad \textbf{(44)}$$

$$D \approx \frac{V_O}{V_{IN}} \qquad \textbf{(45)}$$

$$\overline{I}_L = \overline{I}_O \qquad \textbf{(46)}$$

Figure 64 : Positive-to-Postive Buck Topology

Figure 65: Current when switch: ON
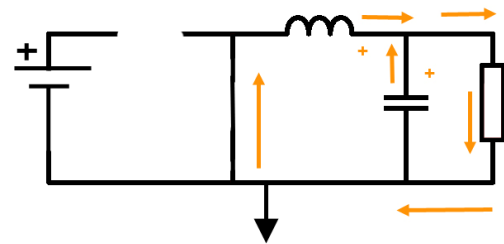
Figure 66: Current when switch: OFF
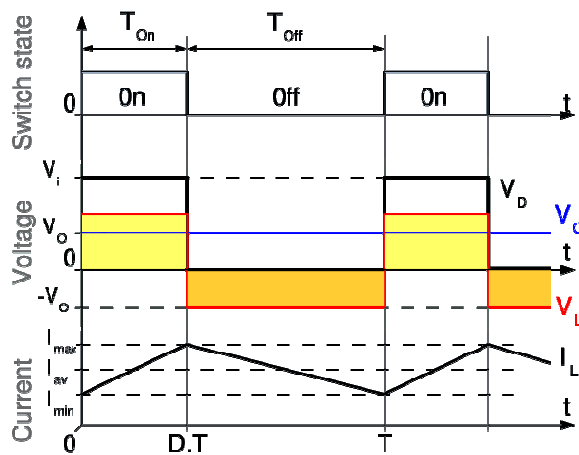
*Figure 67: Time diagrams, provided **C**ontinuous **C**onducting **M**ode.*

A.2.2. Boost Topology

In the basic Boost topology, the inductor is connected to the **input**, so it is characterized by having up conversion, in other words **$V_O > V_{IN}$** while the polarity is also maintained.

In this converter, when the switch is ON, energy from the DC source goes *only* into the inductor (nothing to Z_L), i.e. the current goes through the switch to charge the inductor. There is no conduction by the diode, however when the switch is OFF, energy from both the inductor and the DC source goes to Z_L while current goes through the diode coming from the inductor as it discharges.
The current flow through the capacitor placed at the output is *choppy* (pulsating) when going in and *smooth* at its output having also a null average because the same amount goes in/out on each cycle.

If $\overline{I}_L$ is the average current flowing through the inductor, then the average diode current which only conducts when the switch is OFF, is defined by equation 48 while the average switch current which only conducts when the switch is ON is given by equation 49. Therefore the relations described on equations 50 and 51 are true

$$\overline{I}_{DIODE} = \overline{I}_L \times (1 - D) \qquad \textbf{(47)}$$

$$\overline{I}_{SWITCH} = \overline{I}_L \times D \qquad \textbf{(48)}$$

$$D \approx \frac{(V_O - V_{IN})}{V_O} \qquad \textbf{(49)}$$

$$\overline{I}_L = \frac{\overline{I}_O}{(1 - D)} \qquad \textbf{(50)}$$

Graphically described on Figure 68 to Figure 71 are both the topology and the behavior of this configuration
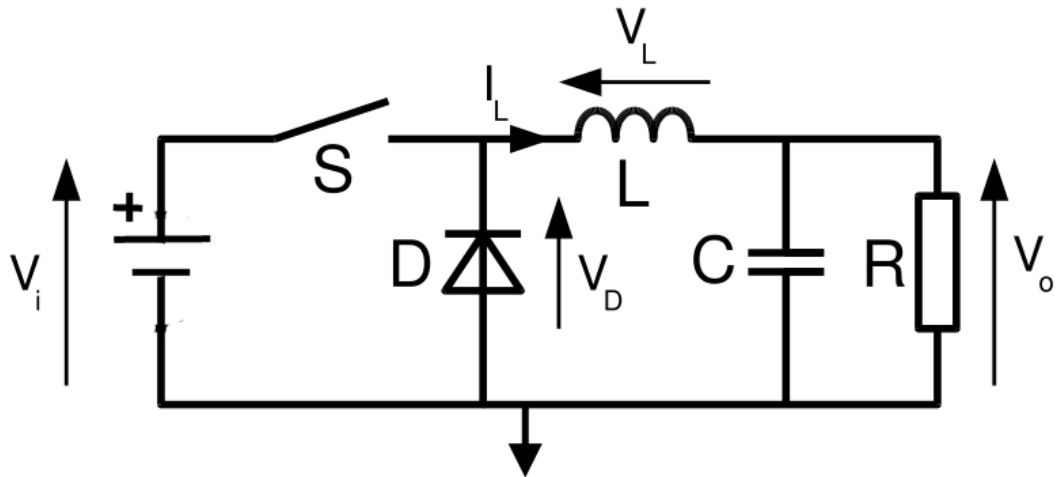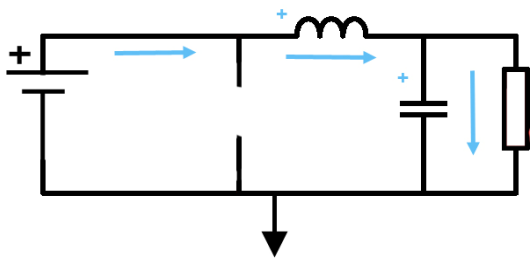
Figure 68: Positive-to-Postive Boost Topology

Figure 69: Current when switch: ON
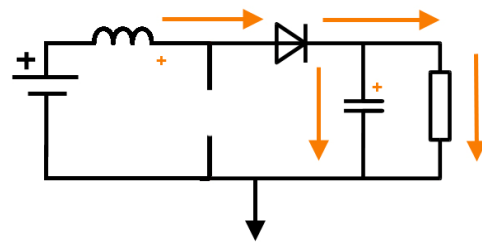
Figure 70: Current when switch: OFF
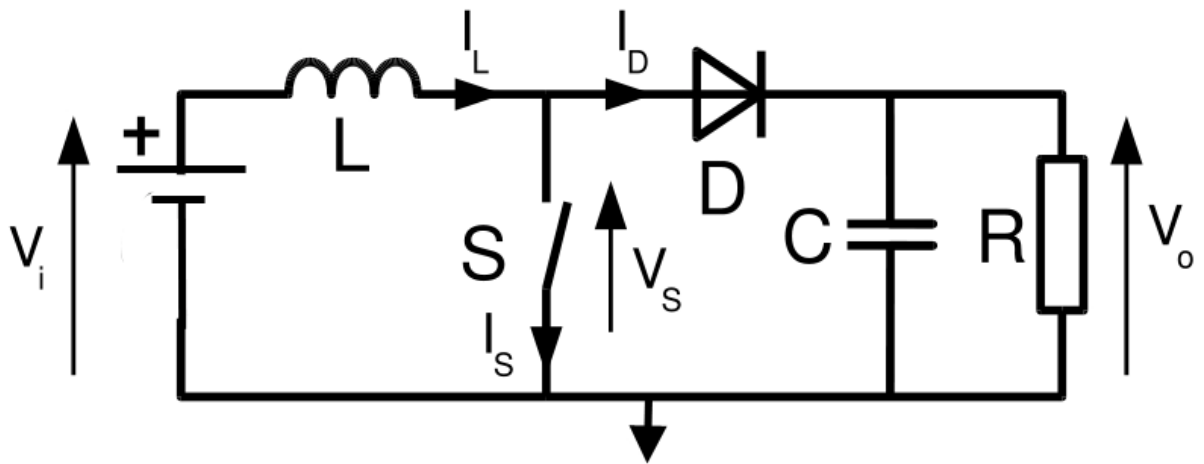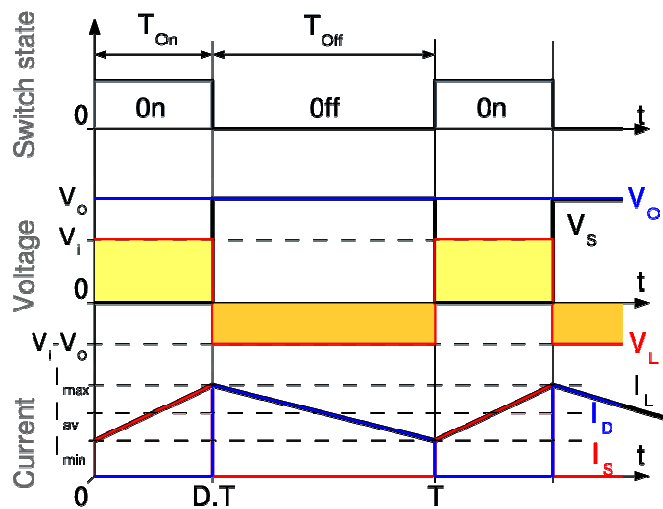

*Figure 71: Time diagrams, provided **C**ontinuous **C**onducting **M**ode.*

A.2.3. Buck-Boost Topology

In the basic Buck-Boost topology, the inductor is connected to the ground, **GND**. One can either have $V_O < V_{IN}$ or $V_O > V_{IN}$ but always with **opposite** polarity ($\Delta\Phi=\pi$).

This generates two possible configurations where the only difference between them is the referencing. GND might be connected either at the terminal with higher voltage of the source or at the lower one. So, the diode is always connected to the inductor's terminal which is not joined to the GND in the adequate direction regarding if the conversion is Positive-to-Negative ($V_O < V_{IN}$) or Negative-to-Positive ($V_O > V_{IN}$).

In this converter, when the switch is ON, energy from DC source only the inductor (nothing to Z_L) while current goes through the switch to charge the inductor, at the same time the energy stored at the capacitor goes to the output. In case it's OFF, only the energy stored at the inductor goes to Z_L while current flows through the diode to discharge the inductor and charge the capacitor.

In case the configuration is *pure flyback*, like the one chosen here, **all** the energy from DC_{IN} to Z_L has been previously stored at the inductor.
The current flow through the capacitor placed at the output is both *choppy* (pulsating) in and out while it has a bull average because the same amount goes in/out on each cycle.

If $\bar{I}_L$ is the average current flowing through the inductor, then the average diode current, since the device only conducts when the switch is OFF, is defined by equation 52 and the average switch current which only conducts when the switch is ON is given by equation 53 so what equations 54 and 55 state is true.

$$\bar{I}_{DIODE} = \bar{I}_L \times (1-D) \qquad \textbf{(51)}$$

$$\bar{I}_{SWITCH} = \bar{I}_L \times D \qquad \textbf{(52)}$$

$$D \approx \frac{V_O}{\left(V_O + V_{IN}\right)} \qquad \textbf{(53)}$$

$$\bar{I}_L = \frac{\bar{I}_O}{(1-D)} \qquad \textbf{(54)}$$

The topology and the behavior of this configuration is graphically described on *Figure* 72 to Figure 75.

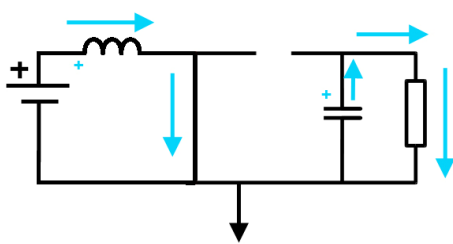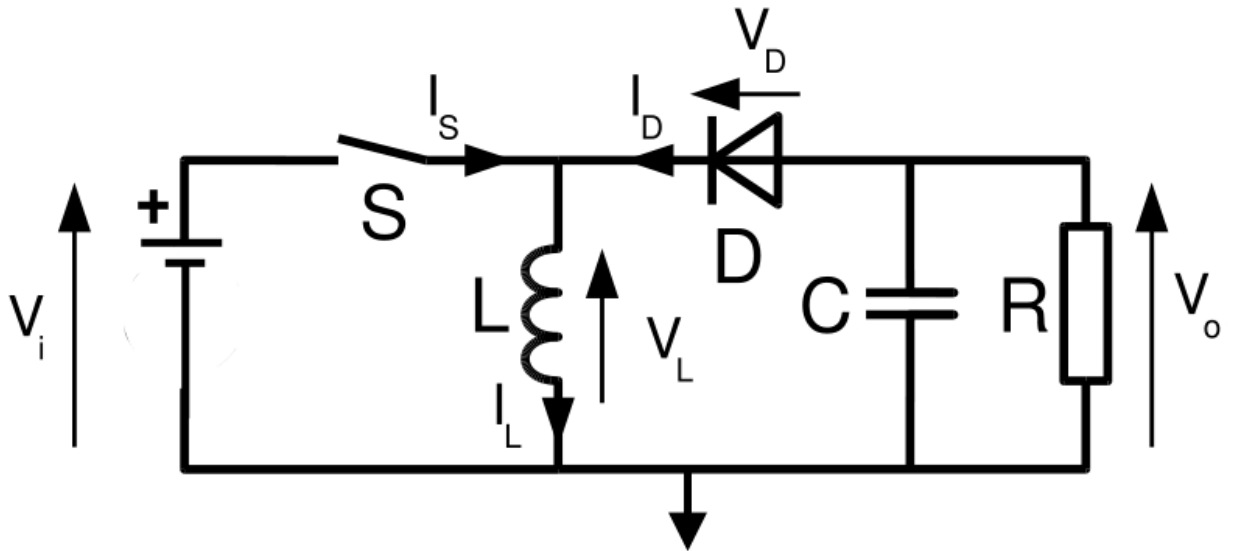*Figure 72: Positive-to-Negative Buck-Boost Topology*
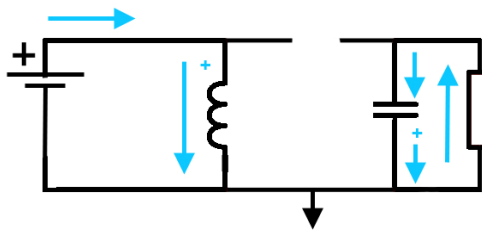
Figure 73: Current when switch: ON   *Figure 74: Current when switch: OFF*
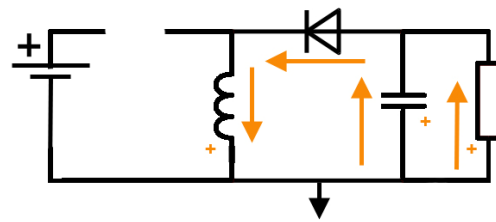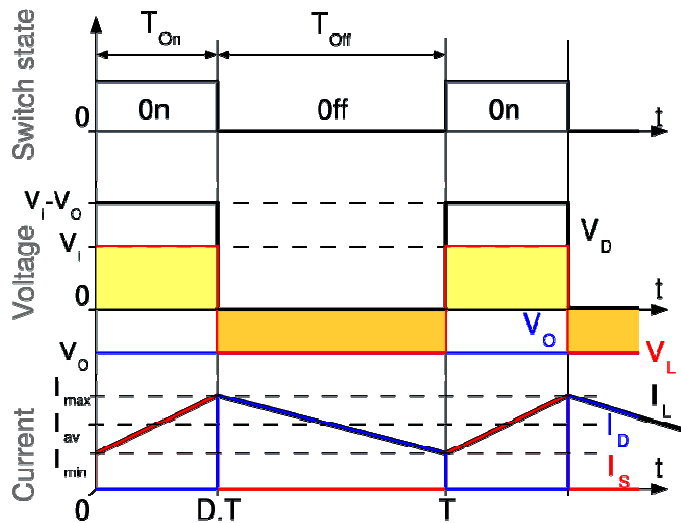
*Figure 75: Time diagrams, provided **Continuous Conducting Mode.***

A.2.4. Final Choice

Since the objective of the design is to transfer <u>as much energy as possible from V_{IN} to V_O</u>, initially the **Buck** where $V_{IN} > V_O$, seems the most logical choice. In this way, the voltage will be reduced because, to inject the maximum power to the circuit, a really huge voltage with a quite low current (to avoid circuitry damage) is going to be placed at the input (of the order of magnitude of approximately 100 V for the input and probably, 5 V for the output {Batteries usually operate with 4-17 V while being charged [10]} while the current will be increased (the *best* for a supercapacitor is to have the highest current possible).

On top of that, since **separability** is the main requirement imposed on the configuration, the coil on the Buck regulator will be replaced by a transformer, leading to what is usually called a **Flyback Converter** operating on Discontinuous Current Mode, DCM, because the current will or will not flow through the coil as a result of the switching. Electrical isolation between the input and the output appears as a consequence of this transformer so that isolation of the control circuit is also a requirement. A feedback signal needs to be provided from the output to the controller which is placed at the primary side, but fortunately with DCM operation, the output voltage is in proportion to the turn-on and reset time of the transformer, **thus the FB voltage can be picked up from a separate sense winding [42]**
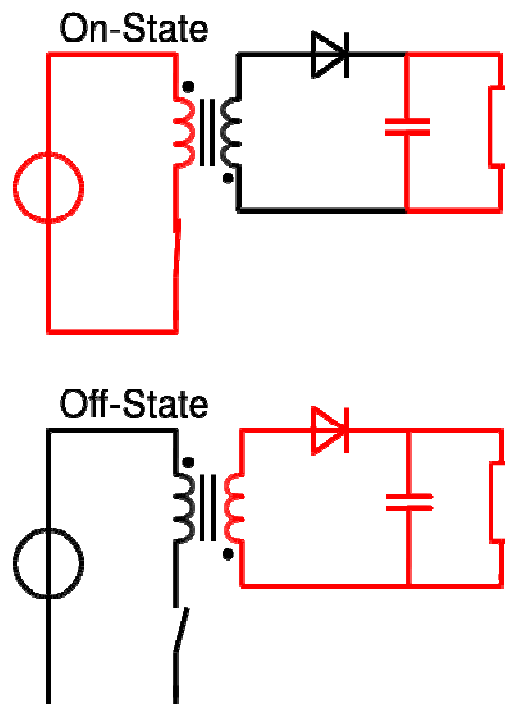
Figure 76: In red, current flow in a flyback converter [42] (switch ON upper, switch OFF lower)
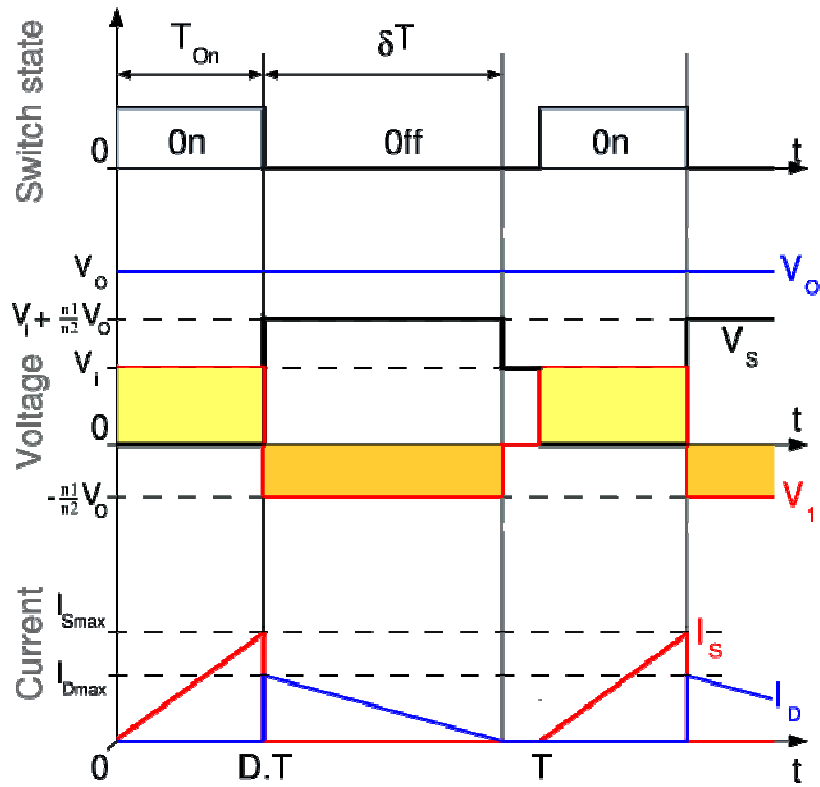
Figure 77: Flyback converter operating on Discontinuous Conduction Mode [42]
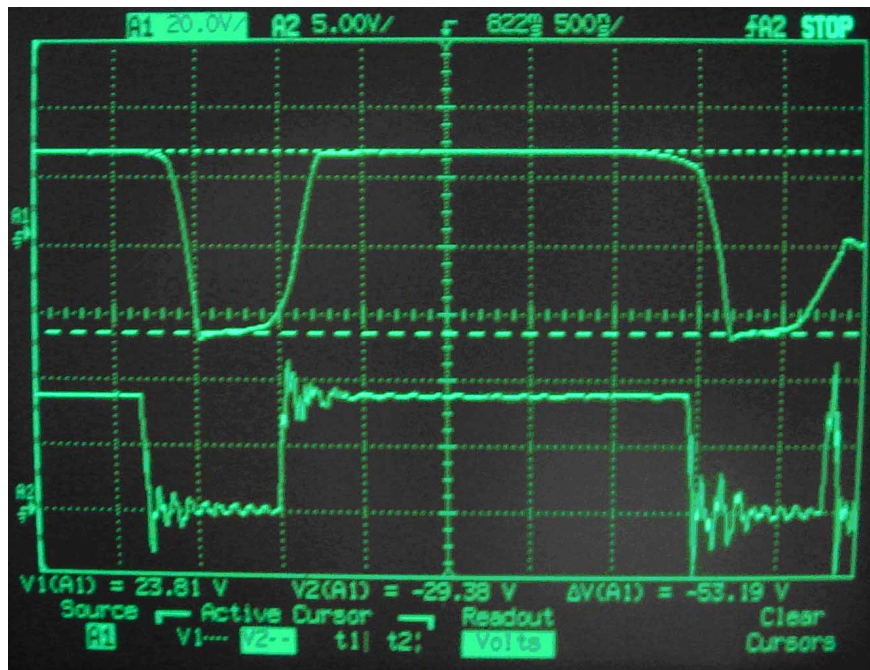
Figure 78: Voltage at the secondary coil (upper) vs V$_{CONTROL\ SWITCH}$ (lower)

Appendix B: Intermediate SPICE results

B.1. Introduction

Although the general procedure to generate a suitable SPICE model of the circuit, our approach, the parts into which the problem was divided, as well as its main results were broadly explained and justified in section 3.2 and chapter 4. of the main body of the thesis, a detailed description of the intermediate stages taking the model from something similar to intusoft's suggestion for a DC-to-DC converter [30] to a version close to that which was implemented is included here in the appendix..

Finally, the *.cir files are also included to complete the detailed description of what was actually simulated.

B.2. First Version: Buck Regulator

As depicted below (for details about the code, see the *.cir file on section B.8.), although some modifications were made from the purposed SMPS which was taken as starting point the main structure is kept so the structure represents a buck regulator (more information about different types of SMPS can also be found at annex A) whose switch is driven by a Current Controlled Mode Pulse Width Modulator.
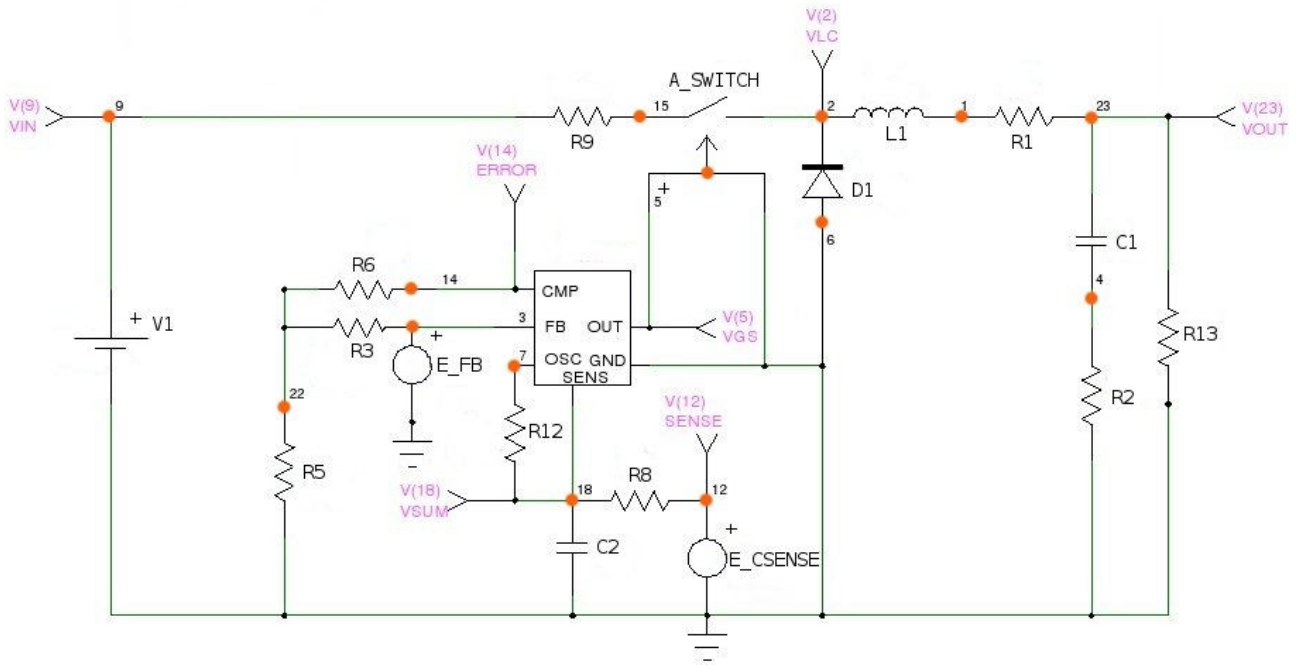
Figure 79: Equivalent circuit of the Buck regulator which was simulated

Node numbering and element names are the same as used in the simulation files to achieve an easier understanding of simulation outputs. In Figure 80, we see the convergence of both output voltage, V(23), and output of the error amplifier, V(14), occur after roughly 300us. The output voltage reaches 5V because the V_{REF} was chosen to 2.5V, thus the CCMPWM will regulate the V_{OUT} observed through FB to twice the value of V_{REF} (as a result of the internal implementation of the error amplifier).
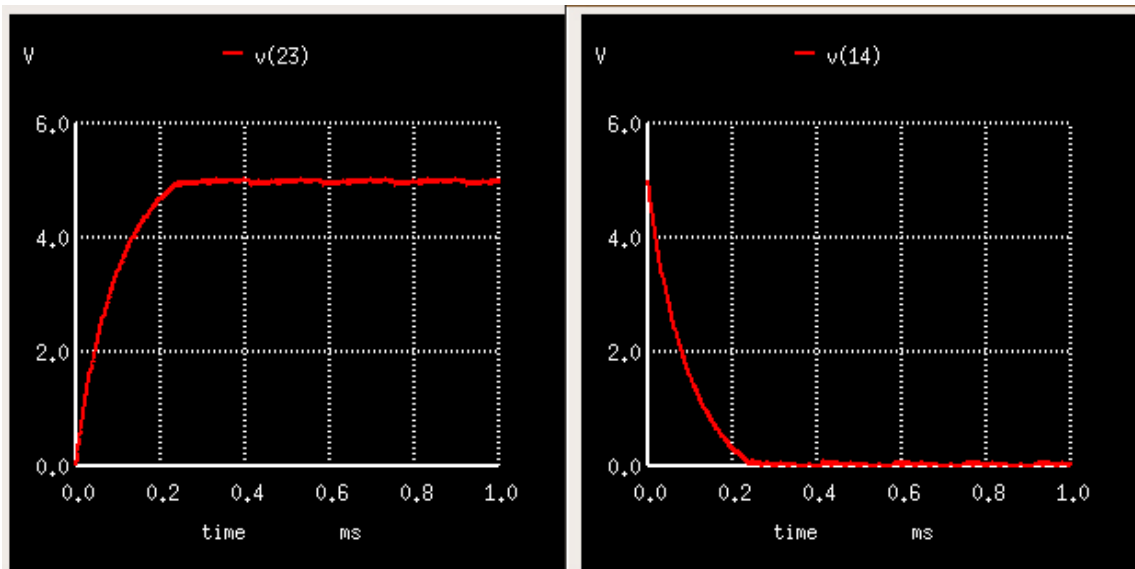
Figure 80: V_{OUT} convergence to 2xV_{REF} (left); V_{ERROR} returns to zero when V_{OUT} is regulated (right)

B.3. Second Version: SMPS with the addition of a secondary winding

As next step (for details about the code, see the *.cir file on section B.9.), the circuit was slightly modified, this represented a huge change since magnetic coupling between two coils (i.e. the transformer implementation) was introduced, leading to a SMPS with two electrically isolated independent parts (regardless of the FeedBack voltage path where a **virtual connection** transmitting V_{OUT} information to FB is still kept, an issue to be solved in subsequent steps). In order to achieve this, an ideal transformer was used instead of a coil. Thus a flyback converter [42] was simulated, which is closer to the final objective as we can see in Figure 81.

Although ideal transformers are not found in the real world, ngspice has a prebuilt coupled-coil model especially designed to be used with a core model. This means that provided a supplier's description of the behaviour of the core (either an array showing the corresponding pairs of B and H, as well as its magnetic area and length, or some values to describe its hysteresis behaviour) it can be easily placed between the primary and secondary side to simulate the circuit's behaviour.
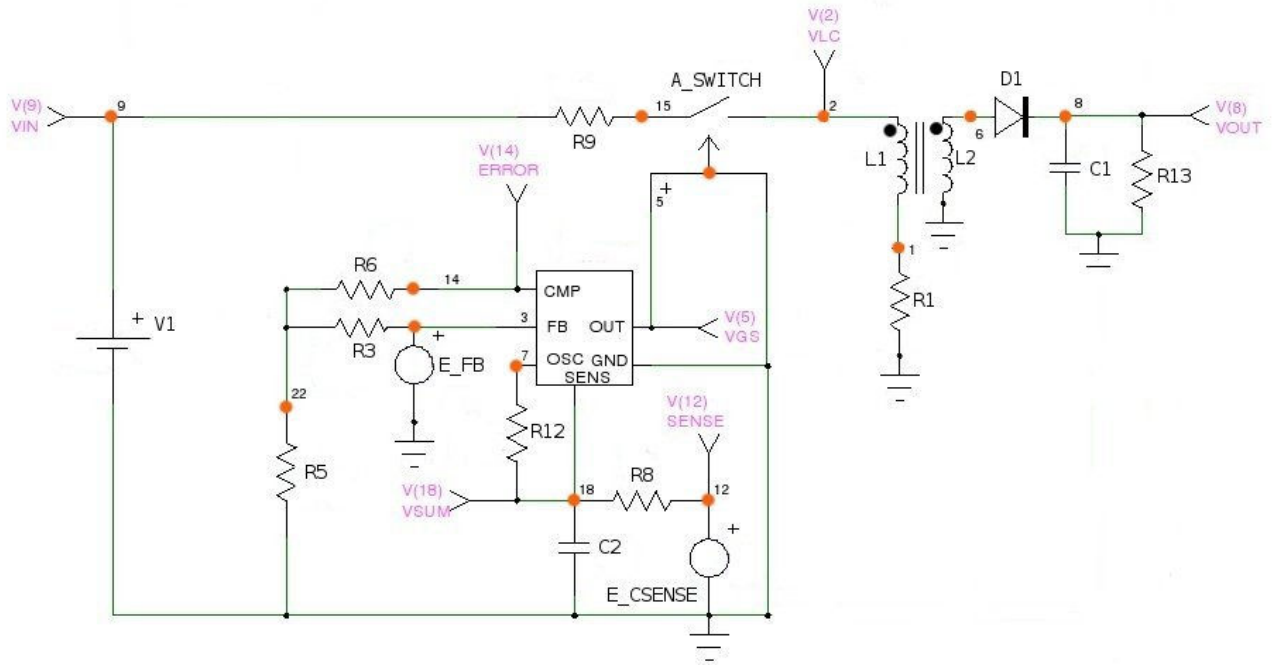
Figure 81 : Equivalent circuit of the simulated flyback converter
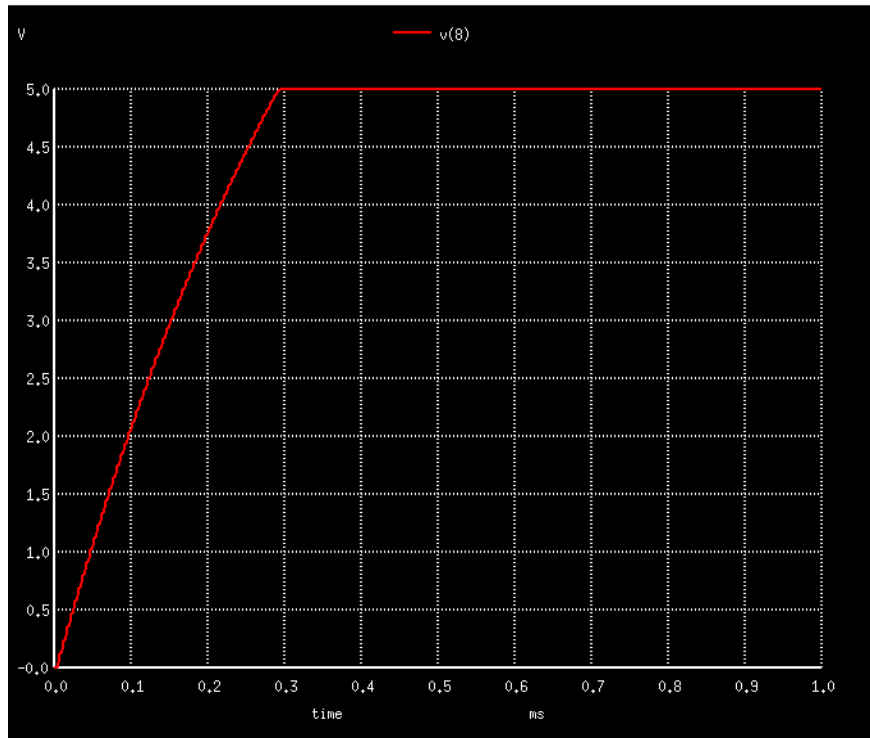
Figure 82: Convergence at the output of the Flyback Converter

As depicted in Figure 82, the behaviour of the circuit is equivalent to the previous one. Only one modification was made in the Schottky diode model in order to achieve convergence of the solution and avoid problems with ngspice: Instead of stating a finite value for the reverse breakdown voltage (BV) it was removed from the model, allowing ngspice to take the default value which was infinite.

Placing the diode series (instead of in parallel) with the switching node, some problems arose as a result of **simulated**, but not real huge voltage values that result from the calculations done during switching between conducting/not-conducting state corresponding to the magnetic field collapsing.
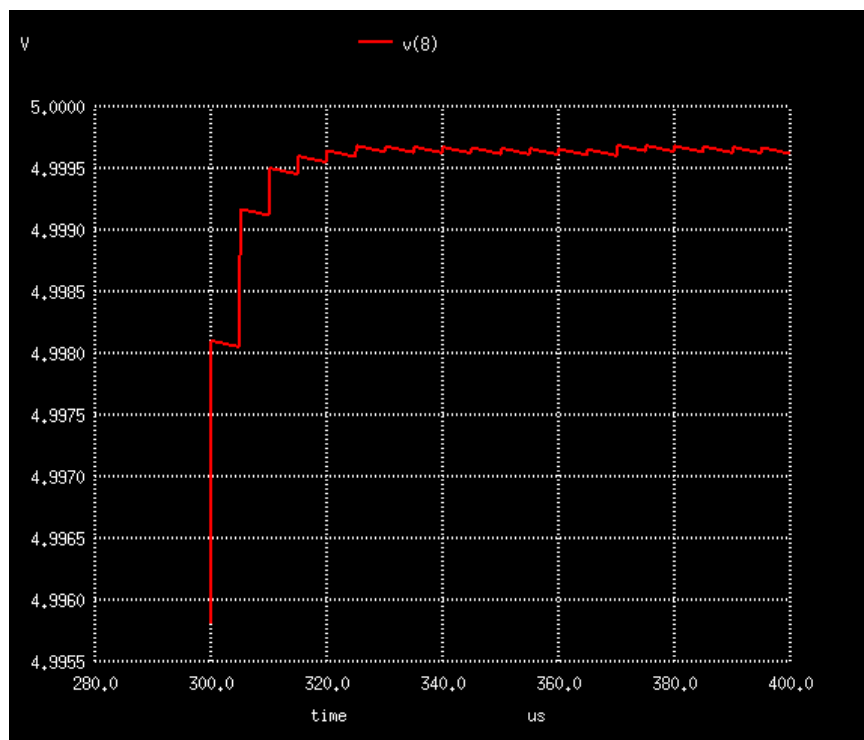
Figure 83 : Regulated output of the flyback converter, constant average with controlled ripple

The objective of Figure 83 is to illustrate that even when the steady-state is achieved, a ripple whose peak-to-peak amplitude can be controlled by modifying the rate between E_CSENSE and the gain of ERRAMP is mantained, as it was explained on section 4.1.2.

B.4. Third Version: SMPS with the addition of a tertiary winding

As an intermediate step between the previous and the final version (for details about the code, see the *.cir file on section B.10.), a tertiary winding was added while the **load** was **doubled** so as **to keep constant** the electrical performance. The coupling between different sides of the transformer is chosen to be 1 and the coils on each arm are exactly the same, hence the current is mirrowed on every arm because the points are electrically equivalent. This is the easiest way to see that the circuit will keep on working exactly in the same way even if a secondary buck is placed in parallel, as it was done in the circuit purposed by MAXIM to build a SMPS with MAX5068E where this tertiary winding was used to provide supply voltage to the integrated circuit (see datasheet on [33]).
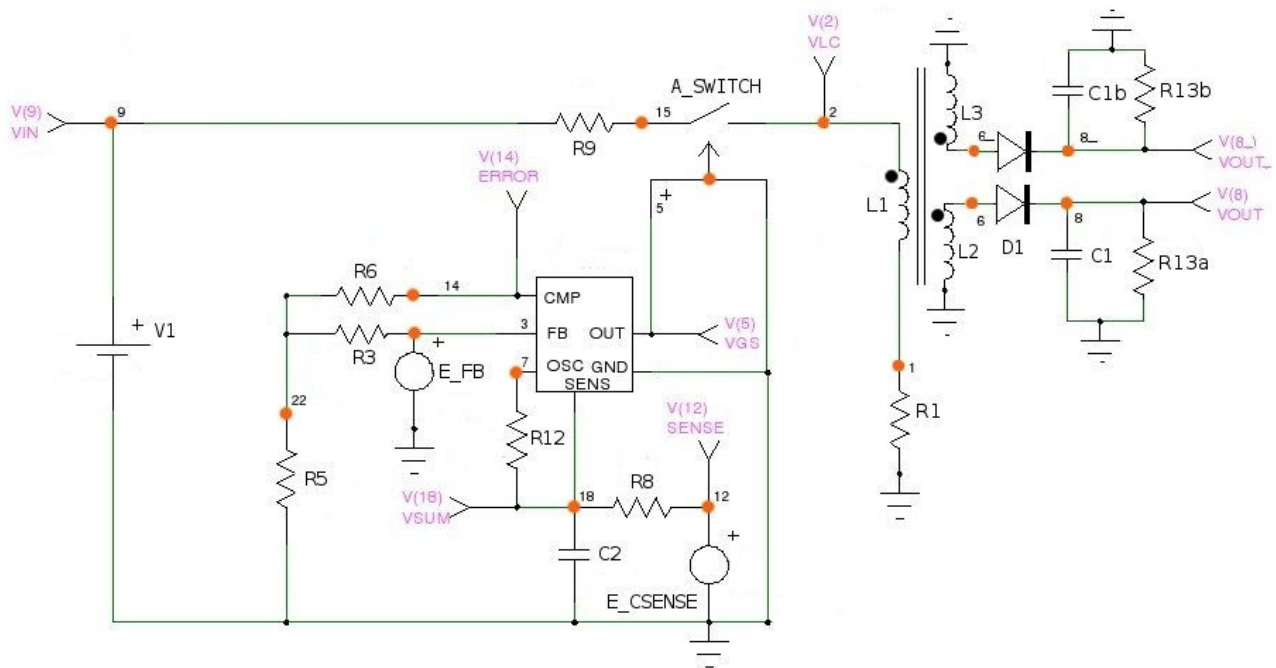
Figure 84: Flyback converter with three arms

As seen in previous versions, there **was still something missing concerning the implementation of two totally isolated parts** that will be placed in two different devices not connected to each other in any other way than the magnetic field of the transformer: **The FB path,** which implemented as a dependent source, **involved a connection between the output and the fixed part of the circuit.**

However, this problem is solved by the addition of the extra winding that will be placed at the fixed part of the SMPS. The output voltage of this tertiary coil will be measured there, generating the necessary feedback information (V_{FB}) information.

Since the **current is mirrowed in both tansformer sides through the shared magnetic field, that it's to say that, provided regulation on one side, regulation on the other will also take place**, maybe with different voltage levels as a result of N_T/N_S ratio, but still regulation.That's the way the CCMPWM is *fooled* and some kind of regulation is achieved in the secondary without the need for a direct feedback path linking the handheld device and the fixed part in the turnstile.

B.5. Final Version: SMPS with the addition of a tertiary winding and a bigger capacitor

In this case a SMPS with the control loop embedded in the fixed primary part leading to a completely isolated topology is built (for details about the code, see the *.cir file on section B.11.). Finally, the capacitor and the load placed on the secondary side are replaced by the real load: a (super)capacitor. This are sensitive devices requiring control in the maximum voltage to avoid damage what could be accomplished by chossing the right turns ratio between the Primary and the Tertiary side:

- N_P/N_S must be adequate to keep a suitable value at V_{IN} (this is also used for output regulation).
- N_P/N_T calculated to maintain the maximum voltage below the Super Capacitor's maximum applied voltage.

So the CCMPWM is still being *cheated* and regulation kept without the need of a feedback path linking the handheld device and the part at the turnstile.
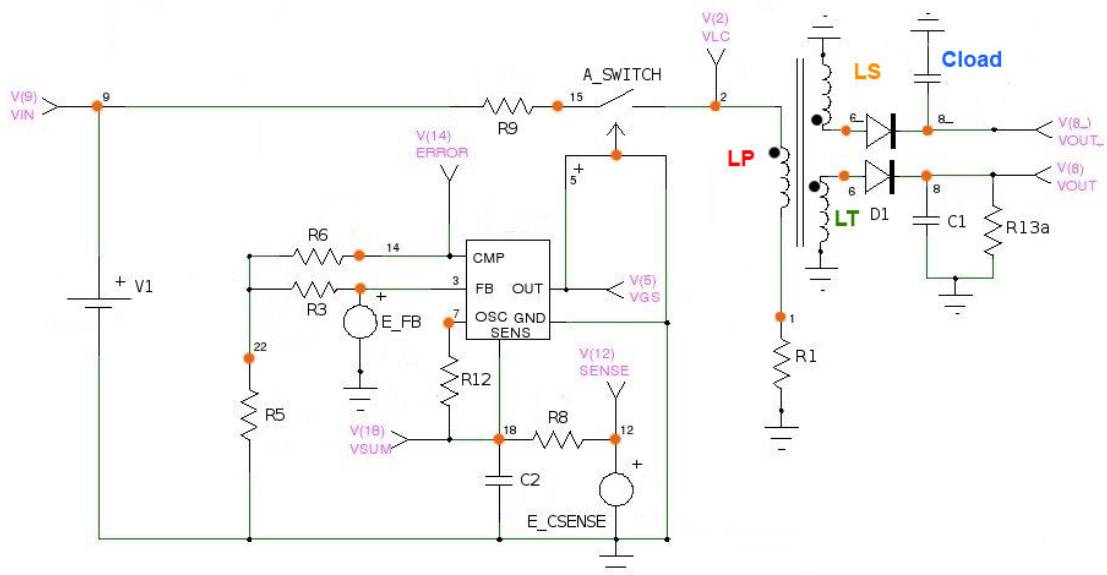
Figure 85: Built circuit's simulation schematic

B.6. sources.cir

.SUBCKT SOURCES clk_+   ramp_+   duty_+ 0
* PARAM:
* Period = 200us
* Ramp = 5V
* DutyMax = 0.5 because Vo/Vin = 6/11.5 = 0.5

Vclk clk_+ 0 pulse(0V 5V 0us 1ns 1ns 100ns 5us)
Vramp ramp_+ 0 PWL(
+ 0 0V
+ 5us 5V
+ 5001ns 0V
+ 10us 5V
+ 10001ns 0V
…
+ 2000us 5V)
Vduty duty_+ 0 pulse 0V 5V 2.5us 1ns 1ns 2.498us 5us
.ENDS SOURCES

B.7. CCMPWM.cir

.SUBCKT CCMPWM CMP FB OSC SENSE OUT OUT_comp

.INCLUDE /home/claudia/sources.cir

X_sources   CLK   OSC   DUTY 0   Sources

_ SR-Latch :
----

a_adc [CLK OUT_comp DUTY] [p_s p_r p3_reset] adc_buff
.model adc_buff adc_bridge(in_low = 0.2V in_high = 3.5V)

a_reset [p_r p3_reset] p_reset or
.model or d_or(rise_delay=1E-12 fall_delay=1E-12)

a_nor1 [p_reset p_not_Q] p_Q nor
.model nor d_nor(rise_delay=1E-12 fall_delay=1E-12)

a_nor2 [p_s p_Q] p_not_Q nor2
.model nor2 d_nor(rise_delay=1E-12 fall_delay=1E-12)

a_dac [p_Q] [OUT] dac_buff
.model dac_buff dac_bridge(out_low=0V out_high=5V out_undef=2V)

X_comp   SENSE CMP OUT_comp   comp

_ Current Comp.

```
---------------------------------------------------------
.SUBCKT COMP        1       2       3
*               (+)     (-)     OUT
B0 4 0 V=uramp(V(1)-V(2))

B1 3 0 V=5*V(4)/(V(4)+0.0000001)

.ENDS COMP
---------------------------------------------------------
```

*X_erramp   +_Vref FB   CMP   erramp

X_erramp   +_Vref FB   CMP   erramp

* CMP is the error amplifier output!!!

Vreference   +_Vref 0 2.5V

*Vref = Desired_Vout/2 --> We set the output value through Vref

_ Error Amplifier

```
---------------------------------------------------------
.SUBCKT ERRAMP     1       2       3
*               +       -       OUT
E1 4 0 1 0 1
E2 3 0 5 0 2
B0 5 0 V=uramp(V(4)-V(2))


.ENDS ERRAMP
---------------------------------------------------------
```

.ENDS CCMPWM

B.8. bucktestccm.cir

Buck Test of CCM PWM

.INCLUDE /home/claudia/CCMPWM.cir

*X_CCMPWM CMP	FB	OSC	SENSE	OUT	OUT_comp	CCMPWM
X_CCMPWM 14	3	7	18	5	25	CCMPWM

```
R6 22 14 220K
C2 18 0 10p
R12 18 7 200Kohm
* Bigger resistor placed in order to reduce sawtooth amplitude
R8 18 12 1Kohm
E1 12 0 1 23 0.5
```

R3 22 3 220kohm
E_FB 3 0 23 0 0.5
R5 22 0 12.94Kohm

R_aux_OUT_comp   25 0 1kohm

V1 9 0 11.5V
R9 9 15 193mohm
A_switch 5 (15 2) switch
.model switch aswitch(cntl_off=0 cntl_on=4 r_off=1e4 r_on=1m log=FALSE)
* With LOG=FALSE the switch works PERFECTLY with a load of 1ohm at 200KHz

X_schottky 0 2 schottky
.SUBCKT schottky d_+ d_-
 D1 d_+ d_- Schottky_low_V_region
 .model Schottky_low_V_region D (IS = 1E-14 RS = 4 N = 1 CJO = 160f XTI = 2 BV = 15)
.ENDS

L1 2 1 4.33u IC=0
R1 1 23 4.5mohm
C1 23 4 50u IC=0
R2 4 0 16mohm
R13 23 0 5
*Bigger load faster

.TRAN 1us 300us 280us 1us
*.TRAN 1ms 1ms 0ms 1us
*.OPTIONS RELTOL=.01
*.OPTIONS ITL4=500
.END

B.9. sec_W.cir

Modifications, First Step: Secondary Winding Addition

.INCLUDE /home/claudia/CCMPWM.cir

*X_CCMPWM	CMP	FB	OSC	SENSE	OUT	OUT_COMP	CCMPWM
X_CCMPWM	14	3	7	18	5	25	CCMPWM

R_help_out_comp 25 0 10kohm

C2 18 0 10p
R12 18 7 200Kohm
R8 18 12 1Kohm
E_CSENSE 12 0 1 0 0.25
* Current sense information

R6 22 14 220K
R3 22 3 220kohm

R5 22 0 12.94Kohm

E_FB 3 0 8 0 0.5

V1 9 0 11.5V
R9 9 15 193mohm
A_switch 5 (15 2) switch
.model switch aswitch(cntl_off=0 cntl_on=4 r_off=1e4 r_on=1m log=TRUE)

L1 2 1 4.33u IC=0
R1 1 0 4.5mohm
L2 6 0 4.33u IC=0
K_transformer L1 L2 1

X_schottky 6 8 schottky
.SUBCKT schottky d_+ d_-
 D1 d_+ d_- Schottky_low_V_region
 .model Schottky_low_V_region D(Is=1E-14A Rs=4 CJO=160f XTI = 2)
.ENDS

* Reverse Breakdown Voltage (BV) is removed because it generated problems as a result of the initial conditions at the sim.

R13 8 0 10kohm
C1 8 0 50u IC=0

*.TRAN 1us 3ms 0ms 1us
*.TRAN 1ms 1045us 1040us 1us
*.TRAN 1ms 1050us 1030us 1us
.TRAN 1ms 400us 300us 1ns
*.OPTIONS RELTOL=.01
*.OPTIONS ITL4=500

.END

B.10. ter_W.cir

Modifications, Third Step: Tertiary Winding Addition

.INCLUDE /home/claudia/CCMPWM.cir

*X_CCMPWM	**CMP**	**FB**	**OSC**	**SENSE**	**OUT**	**OUT_COMP**	**CCMPWM**
X_CCMPWM	**14**	**3**	**7**	**18**	**5**	**25**	**CCMPWM**

R_help_out_comp 25 0 10kohm

C4 18 0 10p
R12 18 7 200Kohm
R8 18 12 1Kohm
E1 12 0 1 0 0.25
* Current sense information

R_CMP_FB 22 14 220K

```
R7 22 3 220kohm
R11 22 0 12.94Kohm


E_FB 3 0 8 0 0.5


V1 9 0 11.5V
R9 9 15 193mohm
A_switch 5 (15 2) switch
.model switch aswitch(cntl_off=0 cntl_on=4 r_off=1e4 r_on=1m log=TRUE)


L1 2 1 4.33u IC=0
R1 1 0 4.5mohm
L2 6 0 4.33u IC=0
K_transformer L1 L2 1


X_schottky 6 8 schottky
.SUBCKT schottky d_+ d_-
 D1 d_+ d_- Schottky_low_V_region
.model Schottky_low_V_region D(Is=1E-14A Rs=4 CJO=160f XTI = 2)
*.model Schottky_low_V_region D(Is=0.1pA Rs=16 CJO=2p Tt=12n Ibv=0.1p)
.ENDS


R13a 8 0 20kohm
* Load is doubled in order to mantain output
C1 8 0 50u IC=0


* Tertiary arm
--------------------------------------------------------------------
L3 6_ 0 4.33u IC=0
K_transformerb L1 L3 1
K_transformerc L2 L3 1


X_schottkyb 6_ 8_ schottkyb
.SUBCKT schottkyb d_+ d_-
 D1 d_+ d_- Schottky_low_V_regionb
.model Schottky_low_V_regionb D(Is=1E-14A Rs=4 CJO=160f XTI = 2)
* .model Schottky_low_V_regionb D(Is=0.1pA Rs=16 CJO=2p Tt=12n Ibv=0.1p)
.ENDS


R13b 8_ 0 20kohm
C1b 8_ 0 50u IC=0
---------------------------------------------------------------------------


*.TRAN 1us 3ms 0ms 1us
*.TRAN 1ms 1045us 1040us 1us
.TRAN 1ms 340us 330us 1us
*.TRAN 1ms 400us 0us 1ns
*.OPTIONS RELTOL=.01
*.OPTIONS ITL4=500


.END
```

B.11. *final.cir*

Modifications Final Step: Circuit Cheating :)

.INCLUDE /home/claudia/CCMPWM.cir

*X_CCMPWM	CMP	FB	OSC	SENSE	OUT	OUT_COMP	CCMPWM
X_CCMPWM	14	3	7	18	5	25	CCMPWM

R_help_out_comp 25 0 10kohm

C4 18 0 10p
R12 18 7 200Kohm
R8 18 12 1Kohm
E1 12 0 1 0 0.25
* Current sense information

R_CMP_FB 0 14 220K
R7 22 3 220kohm
R11 22 0 12.94Kohm

E_FB 3 0 8 0 0.5

V1 9 0 11.5V
R9 9 15 193mohm
A_switch 5 (15 2) switch
.model switch aswitch(cntl_off=0 cntl_on=4 r_off=1e4 r_on=1m log=TRUE)

L1 2 1 4.33u IC=0
R_current_sense 1 0 4.5mohm

X_schottky 2 8 schottky
.SUBCKT schottky d_+ d_-
 D1 d_+ d_- Schottky_low_V_region
 .model Schottky_low_V_region D(Is=1E-14A Rs=4 CJO=160f XTI = 2)
 *.model Schottky_low_V_region D(Is=0.1pA Rs=16 CJO=2p Tt=12n Ibv=0.1p)
.ENDS

R13 8 0 20kohm
C1 8 0 50u IC=0

* Arm placed at the handheld device: No load, but supercapacitor.

L3 6_ 0 4.33u IC=0
K_transformer L1 L3 1

X_schottkyb 6_ 8_ schottkyb
.SUBCKT schottkyb d_+ d_-
 D1 d_+ d_- Schottky_low_V_regionb
 .model Schottky_low_V_regionb D(Is=1E-14A Rs=4 CJO=160f XTI = 2)
 *.model Schottky_low_V_regionb D(Is=0.1pA Rs=16 CJO=2p Tt=12n Ibv=0.1p)
.ENDS

C_supercap 8_ 0 5 IC=0

```
*.TRAN 1us 3ms 0ms 1us
*.TRAN 1ms 1045us 1040us 1us
*.TRAN 1ms 1150us 1130us 1us
.TRAN 1ms 500us 480us 1ns
*.OPTIONS RELTOL=.01
*.OPTIONS ITL4=500

.END
```

B.12. sourcesimplemented.cir

```
.SUBCKT SOURCES 1 2        3        0
* PARAM:
* Period = 3us
* Ramp = 5V
* DutyMax = 0.75

Vclk  1  0 pulse(0V 5V 0us 1ns 1ns 100ns 3us)
Vramp 2 0 PWL(
+ 0 0V
+ 3us 5V
+ 3001ns 0V
+ 6us 5V
+ 6001ns 0V
...
+ 900us 5V)
Vduty 3 0 pulse 0V 5V 2.5us 1ns 1ns 0.498us 3us

.ENDS SOURCES
```

B.13. CCMPWMimplemented.cir

```
.SUBCKT CCMPWM CMP FB OSC SENSE OUT  OUT_comp

.INCLUDE /home/claudia/sourcesimp.cir

X_sources      CLK   OSC   DUTY 0       Sources
----------------------------------------------------------------------------------

*_* SR-Latch :
----------------------------------------------------------------------------

a_adc [CLK OUT_comp DUTY] [p_s p_r p3_reset] adc_buff
.model adc_buff adc_bridge(in_low = 0.2V in_high = 3.5V)

a_reset [p_r p3_reset] p_reset or
```

.model or d_or(rise_delay=1E-12 fall_delay=1E-12)

a_nor1 [p_reset p_not_Q] p_Q nor
.model nor d_nor(rise_delay=1E-12 fall_delay=1E-12)

a_nor2 [p_s p_Q] p_not_Q nor2
.model nor2 d_nor(rise_delay=1E-12 fall_delay=1E-12)

a_dac [p_Q] [OUT] dac_buff
.model dac_buff dac_bridge(out_low=0V out_high=5V out_undef=2V)

X_comp   SENSE   CMP   OUT_comp   comp

_ Current Comp.

.SUBCKT COMP   1   2   3
*   (+)   (-)   OUT
B0 4 0 V=uramp(V(1)-V(2))

B1 3 0 V=5*V(4)/(V(4)+0.0000001)

* FB aumenta muy rápido, hay mucho error pero es muy negativo entonces debería resetear pero no lo hace

.ENDS COMP
----

*X_erramp   +_Vref   FB   CMP   erramp

X_erramp   +_Vref   FB   CMP   erramp

* CMP is the error amplifier output!!!

Vreference   +_Vref 0 4.5V

*Vref = Desired_Vout/2 --> We set the output value through Vref

_ Error Amplifier

.SUBCKT ERRAMP   1   2   3
*   +   -   OUT
E1 4 0 1 0 1
E2 3 0 5 0 2
B0 5 0 V=uramp(V(4)-V(2))

.ENDS ERRAMP

.ENDS CCMPWM

B.14. implemented.cir

Implemented Circuit

.INCLUDE /home/claudia/CCMPWMimplemented.cir

```
*X_CCMPWM  CMP    FB      OSC     SENSE OUT    OUT_COMP    CCMPWM
X_CCMPWM   14     3       7       18    5      25          CCMPWM
```

R_help_out_comp 25 0 10kohm

C4 18 0 10p
R12 18 7 200Kohm
R8 18 12 1Kohm
E1 12 0 1 0 0.005
* Current sense information

R_CMP_FB 22 14 220K
R7 22 3 220kohm
R11 22 0 12.94Kohm

E_FB 3 0 8 0 0.5
* 8 is the one passing FB information

V1 9 0 24V
R9 9 15 193mohm
A_switch 5 (15 2) switch
.model switch aswitch(cntl_off=0 cntl_on=4 r_off=1e4 r_on=1m log=TRUE)

L1 2_ 1 31.2u IC=0
Raux 2 2_ 3mohm
R1 1 0 50mohm

L2 6 0 30u IC=0
K_transformer L1 L2 1

X_schottky 6 8 schottky
.SUBCKT schottky d_+ d_-
** D1 d_+ d_- Schottky_low_V_region OFF**
.model Schottky_low_V_region D(Is=1E-14A Rs=4 CJO=160f XTI = 2)
*.model Schottky_low_V_region D(Is=0.1pA Rs=16 CJO=2p Tt=12n Ibv=0.1p)
.ENDS

R13a 8 0 200ohm
* 12v, 0.06A --> R = 12/0.06 = 200
* 12V, 5W -----> R = 12*12/5 = 30
C1 8 0 47u IC=0

* Secondary arm
--
L3 6_ 0 118u IC=0
K_transformerb L1 L3 0.5

K_transformerc L2 L3 0.5

*To model the effect of the distance, the coupling is NOT perfect

X_schottkyb 6_ 8_ schottkyb
.SUBCKT schottkyb d_+ d_-
 D1 d_+ d_- Schottky_low_V_regionb OFF
.model Schottky_low_V_regionb D(Is=1E-14A Rs=4 CJO=160f XTI = 2)
* .model Schottky_low_V_regionb D(Is=0.1pA Rs=16 CJO=2p Tt=12n Ibv=0.1p)
.ENDS

C1b 8_ 0 820u IC=0
---

*.TRAN 1us 3ms 0ms 1us
*.TRAN 1ms 1045us 1040us 1us
*.TRAN 1ms 305us 300us 1us
.PLOT V(8_)
.PLOT V(14)

.TRAN 1us 900us 0us 1us

.END

Appendix C: Measured Data

C.1. Values from test#5

C.1.1. Tables from test#5.1: Card with different V_{DC}

N_S [turns]	N_S/N_P	L_{HALF} [μH]	V_{FINAL}	V_C (t_0 = 300ms)	Power [mW] = $CV^2/(2*to)$
100	5,00	735,00	17,91	13,00	230,97
75	3,75	397,30	22,59	16,31	363,56
50	2,50	168,80	25,41	14,56	289,72
40	2,00	118,10	22,12	13,91	264,43
35	1,75	92,40	26,34	12,88	226,72
30	1,50	64,20	27,00	11,62	184,53
25	1,25	50,70	23,81	10,34	146,12
20	1,00	28,50	18,19	8,91	108,40
10	0,50	8,60	13,44	5,59	42,77

Table 16: Data collected in test#5.1 with V_{DC} = 12V

N_S [turns]	N_S/N_P	L_{HALF} [μH]	V_{FINAL}	V_C (t_0 = 300ms)	Power [mW] = $CV^2/(2*to)$
100	5,00	735,00	14,00	9,69	128,27
75	3,75	397,30	18,22	12,12	200,76
50	2,50	168,80	18,53	14,56	289,72
40	2,00	118,10	17,28	13,91	264,43
35	1,75	92,40	21,50	12,88	226,72
30	1,50	64,20	20,09	11,62	184,53
25	1,25	50,70	23,19	10,47	149,82
20	1,00	28,50	18,81	8,91	108,40
10	0,50	8,60	11,06	5,59	42,77

Table 17: Data collected in test#5.1 with V_{DC} = 18V

N_S [turns]	N_S/N_P	L_{HALF} [µH]	V_{FINAL}	V_C (t_0 = 300ms)	Power [mW] = $CV^2/(2*t_0)$
100	5,00	735,00	12,12	7,84	84,09
75	3,75	397,30	16,97	10,00	136,67
50	2,50	168,80	16,34	13,38	244,67
40	2,00	118,10	15,56	13,41	245,77
35	1,75	92,40	15,84	12,81	224,26
30	1,50	64,20	19,78	11,62	184,53
25	1,25	50,70	18,34	10,47	149,82
20	1,00	28,50	16,94	9,22	116,15
10	0,50	8,60	12,94	5,97	48,69

Table 18: Data collected in test#5.1 with V_{DC} = 24V

C.1.2. Tables from test#5.2: 1 Washer with different V_{DC}

N_S [turns]	N_S/N_P	L_{HALF} [µH]	V_{FINAL}	V_C (t_0 = 300ms)	Power [mW] = $CV^2/(2*t_0)$
100	5,00	735,00	23,69	9,72	129,09
75	3,75	397,30	24,16	8,75	104,64
50	2,50	168,80	19,16	8,31	94,42
40	2,00	118,10	24,16	8,50	98,74
35	1,75	92,40	25,53	7,66	80,11
30	1,50	64,20	26,03	7,69	80,78
25	1,25	50,70	18,19	6,91	65,18
20	1,00	28,50	10,53	5,97	48,69
10	0,50	8,60	7,38	3,59	17,65

Table 19: Data collected in test#5.2 with V_{DC} = 12V

N_S [turns]	N_S/N_P	L_{HALF} [μH]	V_{FINAL}	V_C (t_0 = 300ms)	Power [mW] = $CV^2/(2*to)$
100	5,00	735,00	20,72	8,47	98,02
75	3,75	397,30	19,16	9,00	110,70
50	2,50	168,80	17,75	9,06	112,23
40	2,00	118,10	28,22	8,50	98,74
35	1,75	92,40	26,00	8,50	98,74
30	1,50	64,20	21,97	8,31	94,42
25	1,25	50,70	21,62	7,34	73,71
20	1,00	28,50	13,22	6,59	59,42
10	0,50	8,60	7,38	3,59	17,65

Table 20: Data collected in test#5.2 with V_{DC} = 18V

N_S [turns]	N_S/N_P	L_{HALF} [μH]	V_{FINAL}	V_C (t_0 = 300ms)	Power [mW] = $CV^2/(2*to)$
100	5,00	735,00	19,62	7,41	74,96
75	3,75	397,30	17,12	8,69	103,16
50	2,50	168,80	17,75	9,13	113,80
40	2,00	118,10	26,34	9,56	124,96
35	1,75	92,40	24,28	9,25	116,94
30	1,50	64,20	20,75	8,88	107,65
25	1,25	50,70	21,94	8,03	88,15
20	1,00	28,50	13,97	7,22	71,22
10	0,50	8,60	6,13	3,59	17,65

Table 21: Data collected in test#5.2 with V_{DC} = 24V

C.1.3. Tables from test#5.3: 2 Washers with different V_{DC}

N_S [turns]	N_S/N_P	L_{HALF} [µH]	V_{FINAL}	V_C (t_0 = 300ms)	Power [mW] = $CV^2/(2 \cdot t_0)$
100	5,00	735,00	23,22	6,28	53,92
75	3,75	397,30	18,06	5,31	38,56
50	2,50	168,80	17,75	5,34	39,03
40	2,00	118,10	22,44	5,19	36,78
35	1,75	92,40	18,25	5,41	39,94
30	1,50	64,20	12,69	4,91	32,89
25	1,25	50,70	15,53	4,53	28,06
20	1,00	28,50	10,16	4,06	22,55
10	0,50	8,60	4,34	2,25	6,92

Table 22: Data collected in test#5.3 with V_{DC} = 12V

N_S [turns]	N_S/N_P	L_{HALF} [µH]	V_{FINAL}	V_C (t_0 = 300ms)	Power [mW] = $CV^2/(2 \cdot t_0)$
100	5,00	735,00	19,94	5,84	46,67
75	3,75	397,30	19,94	5,50	41,34
50	2,50	168,80	18,53	5,66	43,72
40	2,00	118,10	23,06	5,63	43,24
35	1,75	92,40	19,59	5,50	41,34
30	1,50	64,20	13,81	5,28	38,11
25	1,25	50,70	18,03	5,09	35,46
20	1,00	28,50	14,06	4,56	28,44
10	0,50	8,60	4,53	2,36	7,61

Table 23: Data collected in test#5.3 with V_{DC} = 18V

N_S [turns]	N_S/N_P	L_{HALF} [μH]	V_{FINAL}	V_C (t_0 = 300ms)	Power [mW] = $CV^2/(2*t_0)$
100	5,00	735,00	18,69	5,84	46,67
75	3,75	397,30	21,03	5,81	46,17
50	2,50	168,80	22,59	6,25	53,39
40	2,00	118,10	22,28	6,13	51,27
35	1,75	92,40	20,53	6,00	49,20
30	1,50	64,20	20,44	5,97	48,69
25	1,25	50,70	22,72	5,41	39,94
20	1,00	28,50	15,00	5,25	37,67
10	0,50	8,60	4,09	2,52	8,65

Table 24: Data collected in test#5.3 with V_{DC} = 24V

C.2. Graphs from test#5

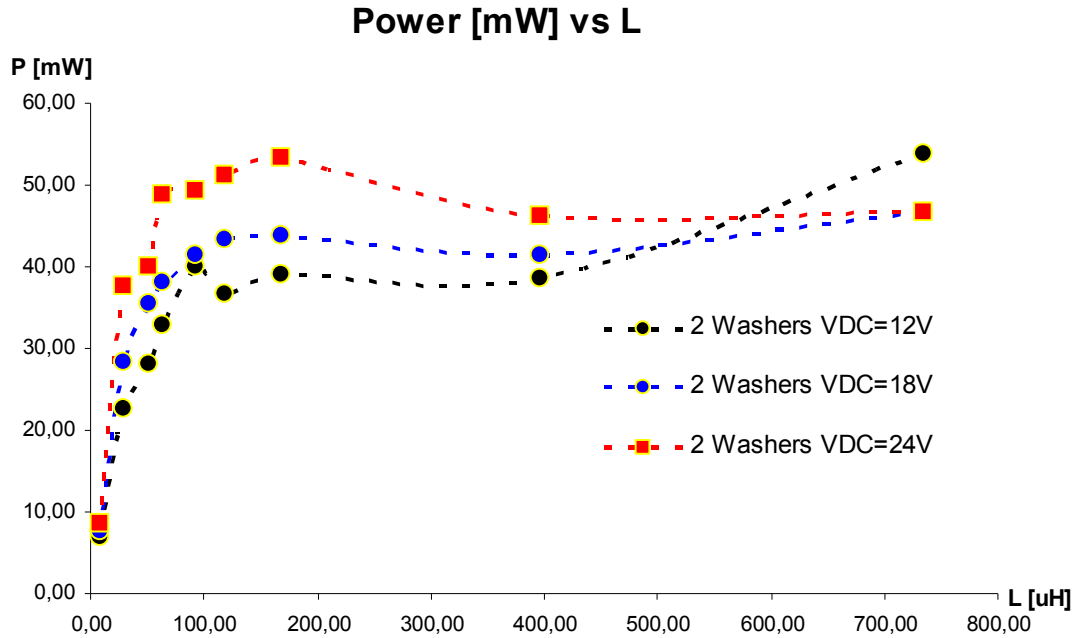## C.2.1. Graphs from test#5.1: Card with different V$_{DC}$
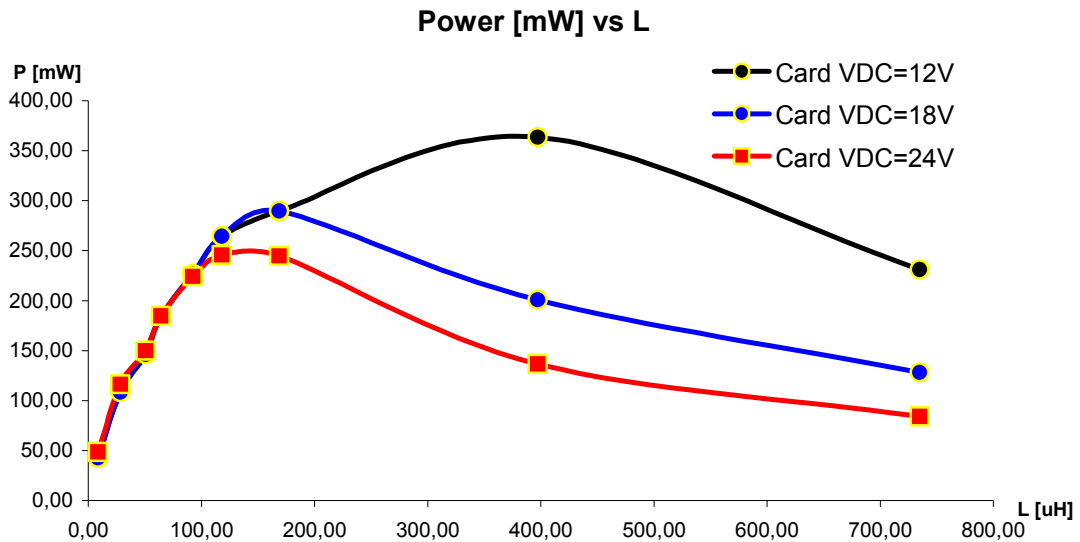
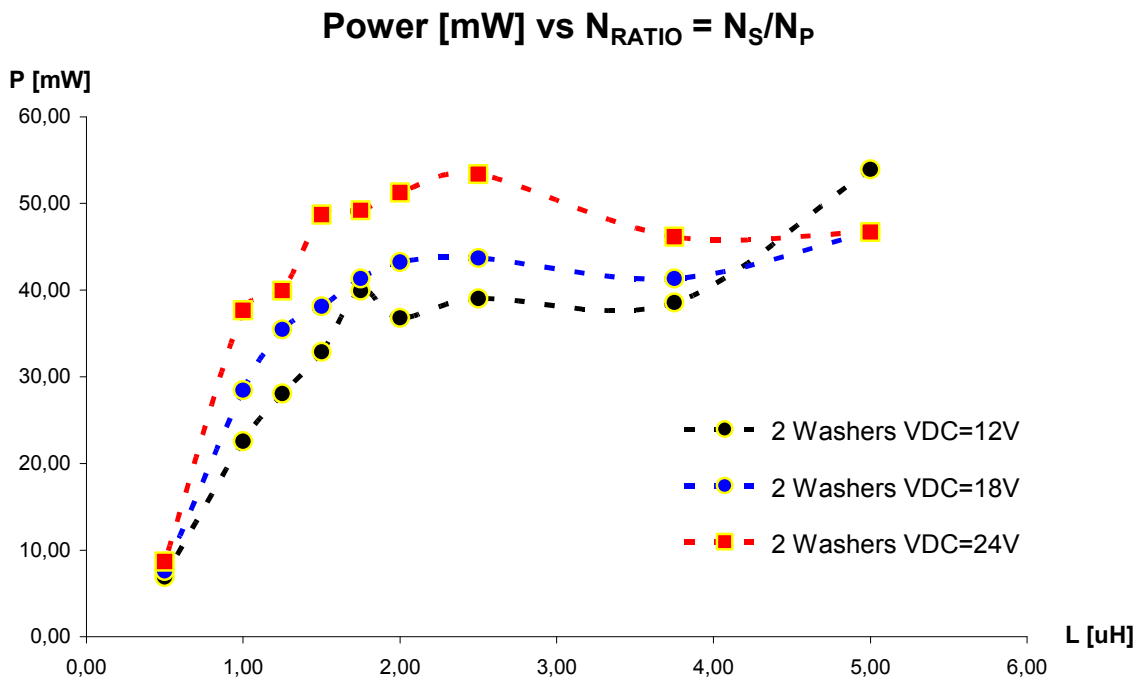*Figure 86: Comparative among data collected in test#51 with different V$_{DC}$*
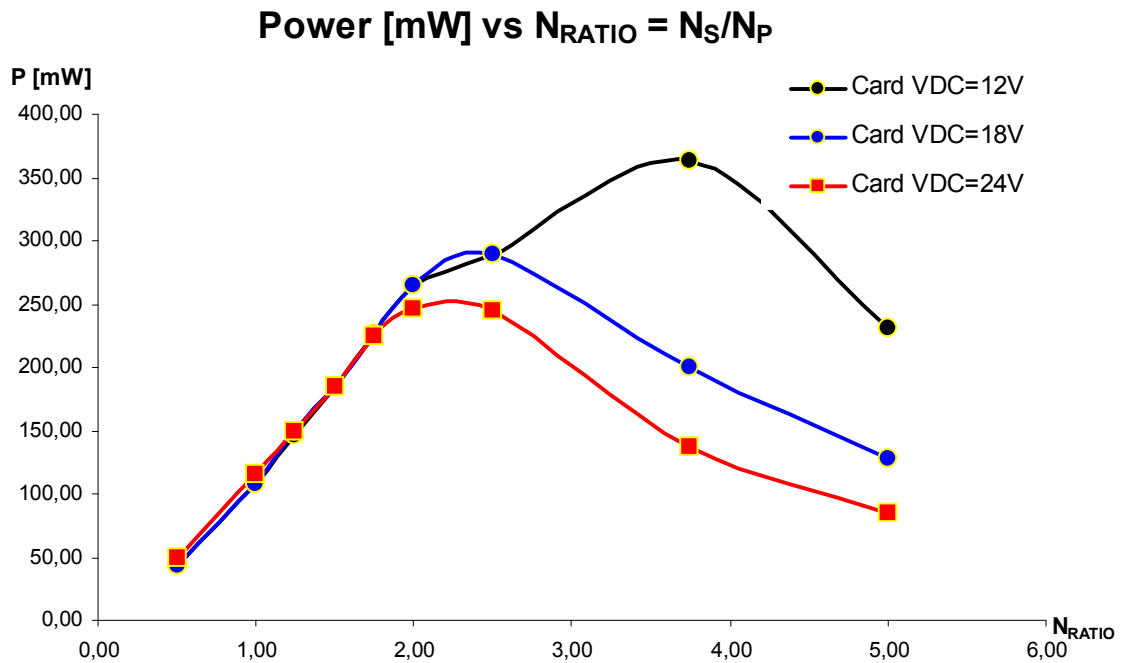
Figure 87: Comparative among data collected in test#51 with different V$_{DC}$

C.2.2. Graphs from test#5.2: 1 washer with different V_{DC}

Power [mW] vs L
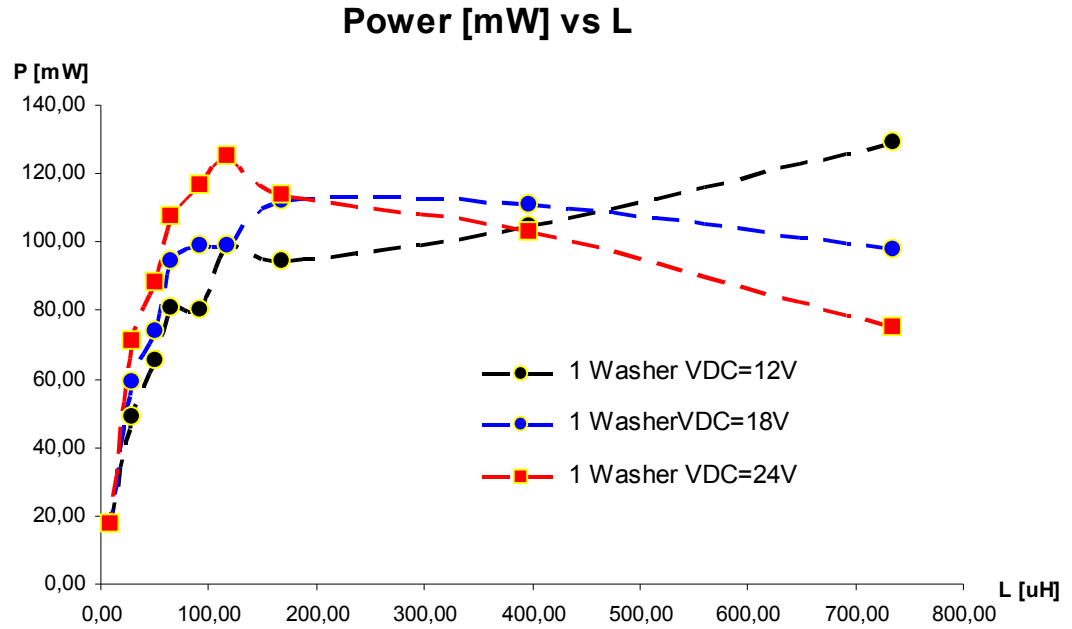
Figure 88: Comparative among data collected in test#52 with different V_{DC}

Power [mW] vs $N_{RATIO} = N_S/N_P$
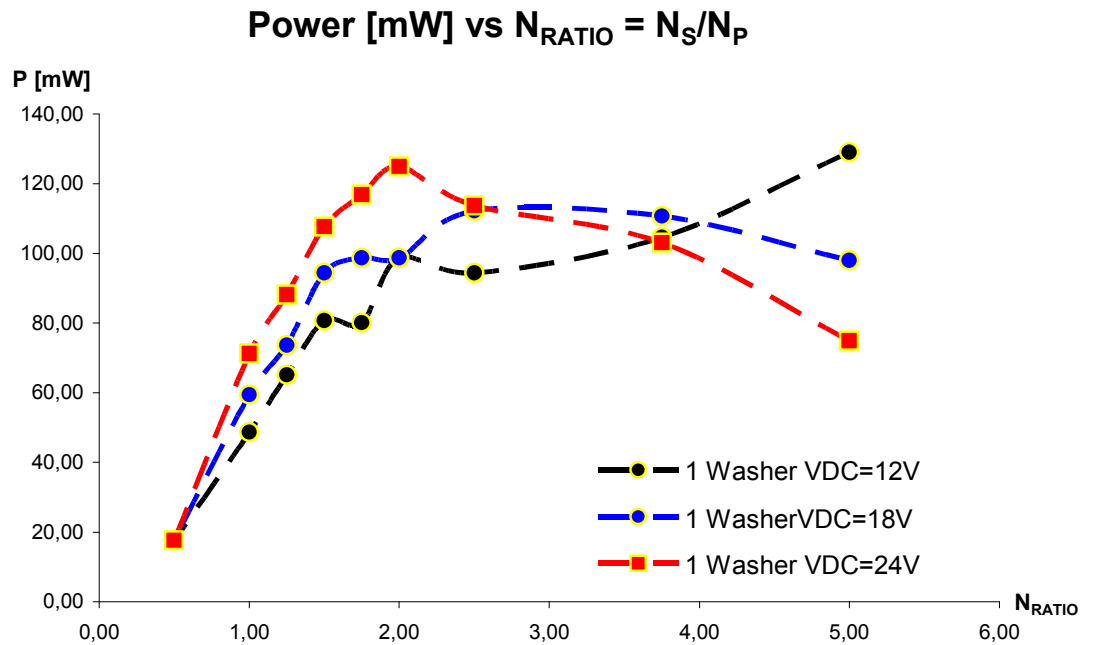
Figure 89: Comparative among data collected in test#52 with different V_{DC}

C.2.3. Graphs from test#5.3: 2 washers with different V_{DC}

Power [mW] vs L

Figure 90: Comparative among data collected in test#53 with different V_{DC}

Power [mW] vs $N_{RATIO} = N_S/N_P$

Figure 91: Comparative among data collected in test#53 with different V_{DC}

C.2.4. Behaviour comparative with V_{DC} = 12V
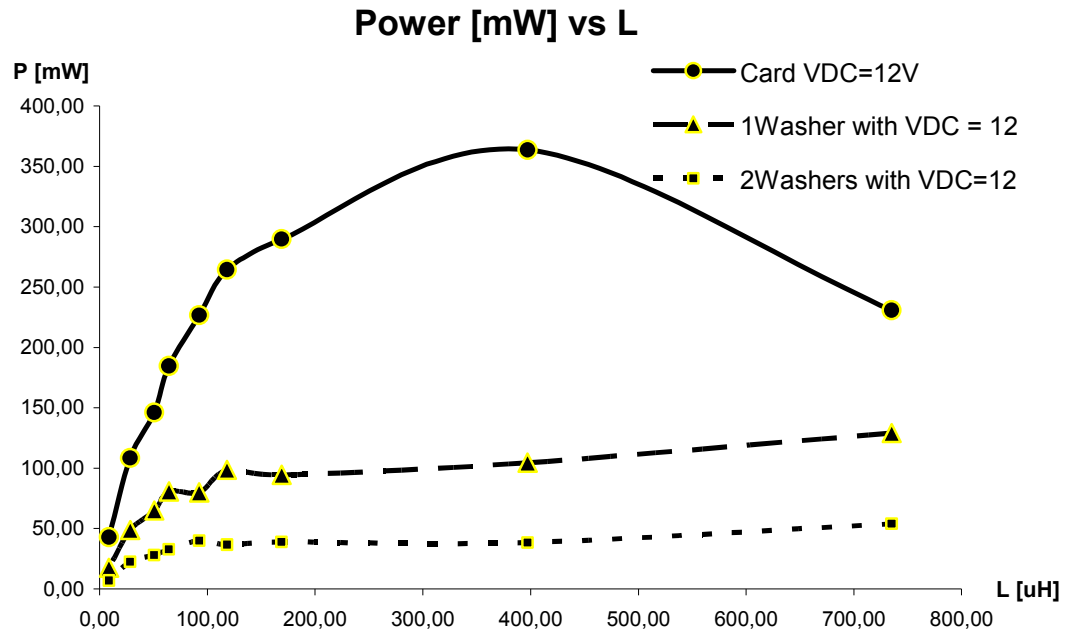
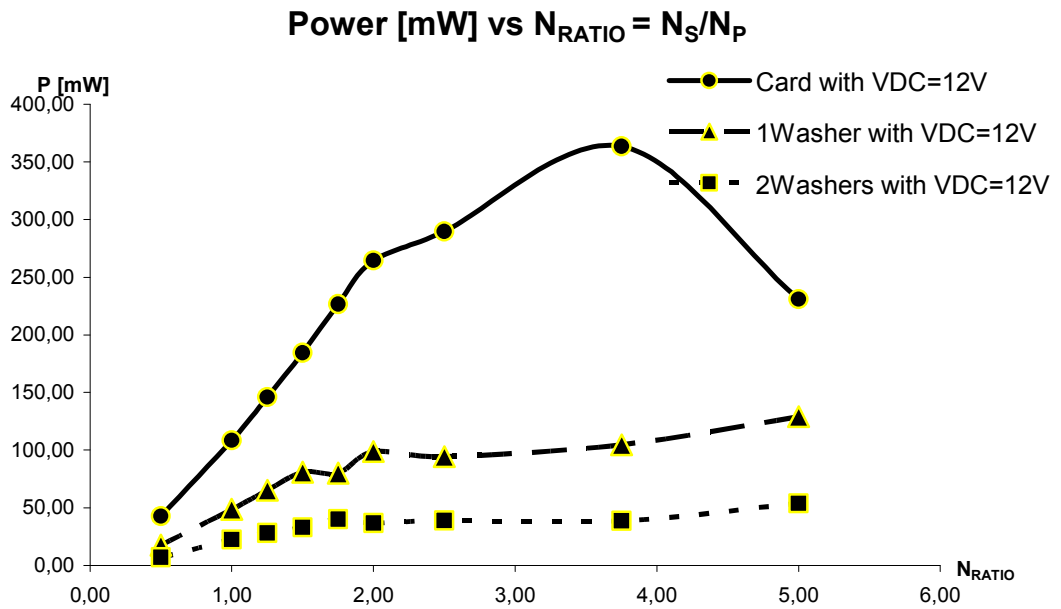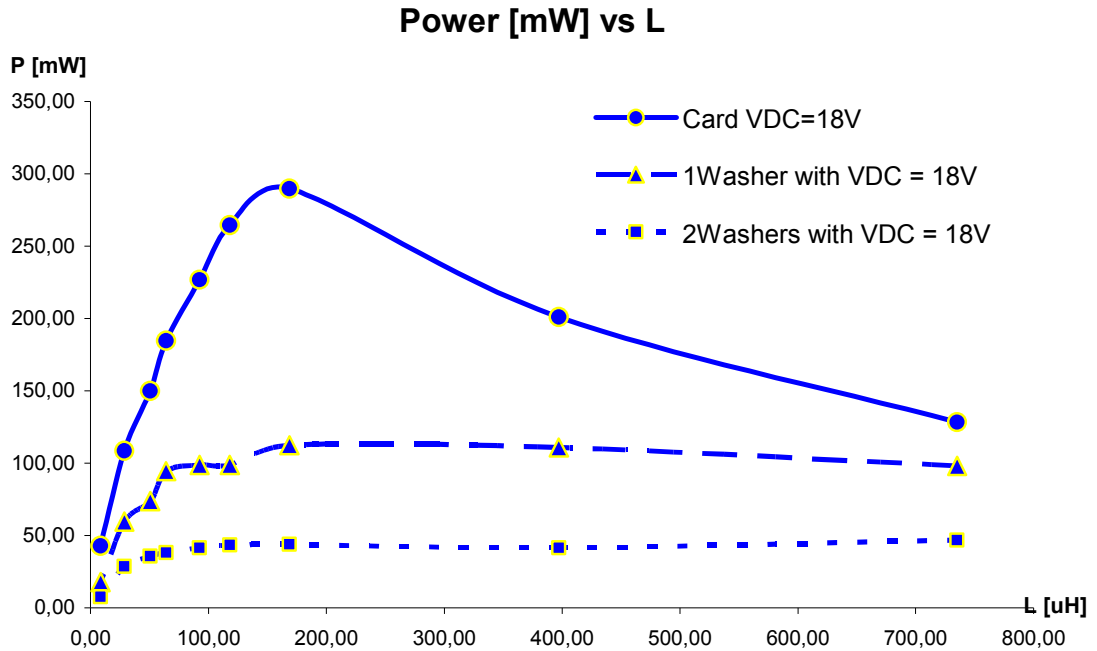*Figure 92: Comparative among data collected in different tests with the same V_{DC} = 12V*
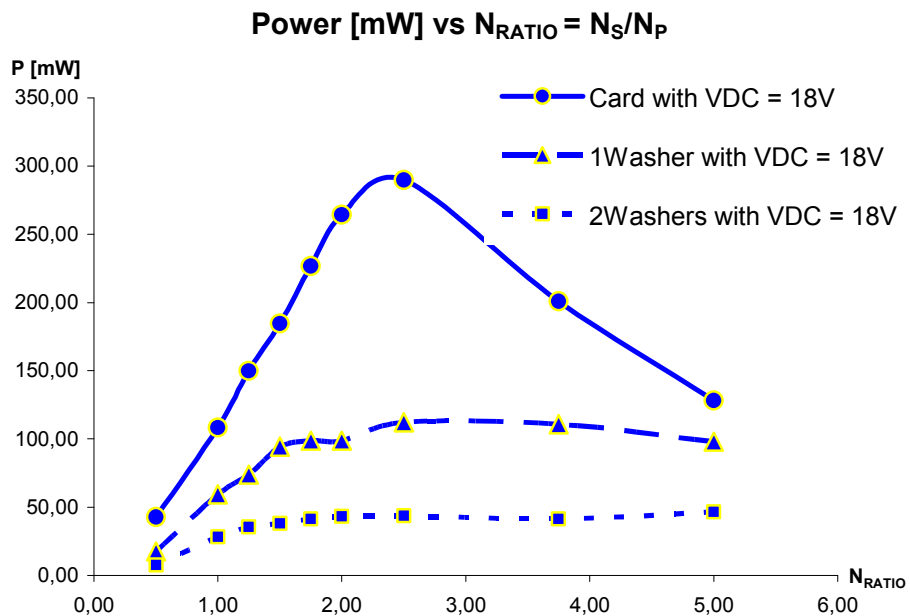

Figure 93: Comparative among data collected in different tests with the same V_{DC} = 12V

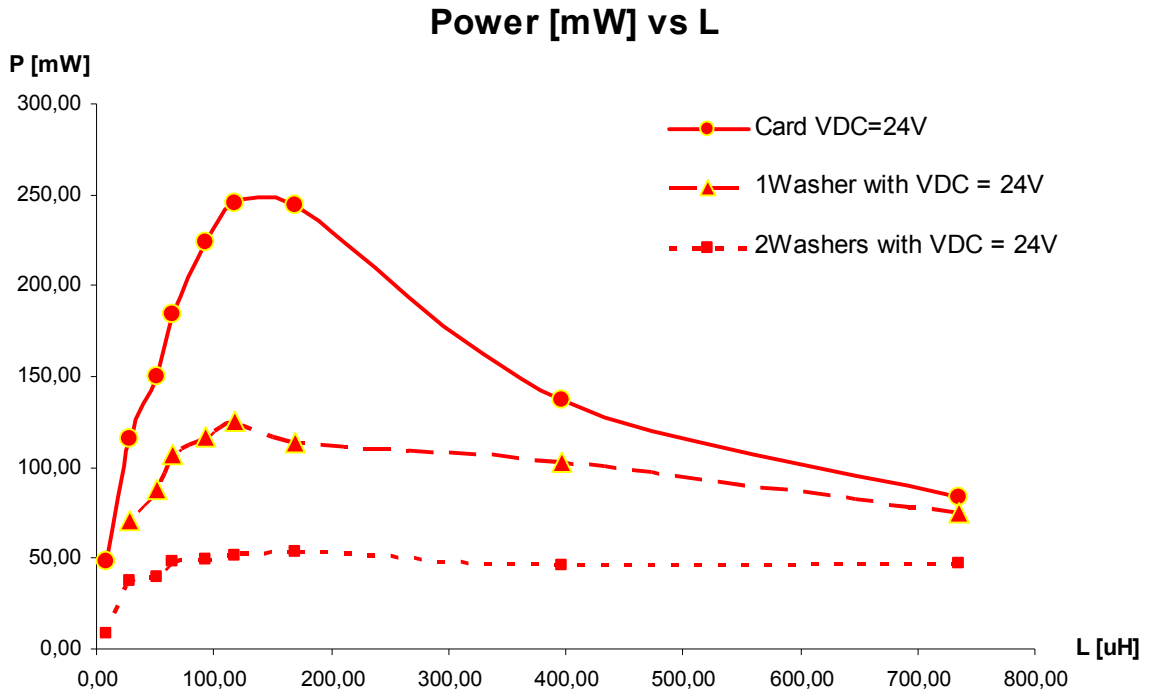## C.2.5. Behaviour comparative with V_{DC} = 18V

Figure 94: Comparative among data collected in different tests with the same V_{DC} = 18V

Figure 95: Comparative among data collected in different tests with the same V_{DC} = 18V

C.2.6. Behaviour comparative with V_{DC} = 24V

Figure 96: Comparative among data collected in different tests with the same V_{DC} = 24V
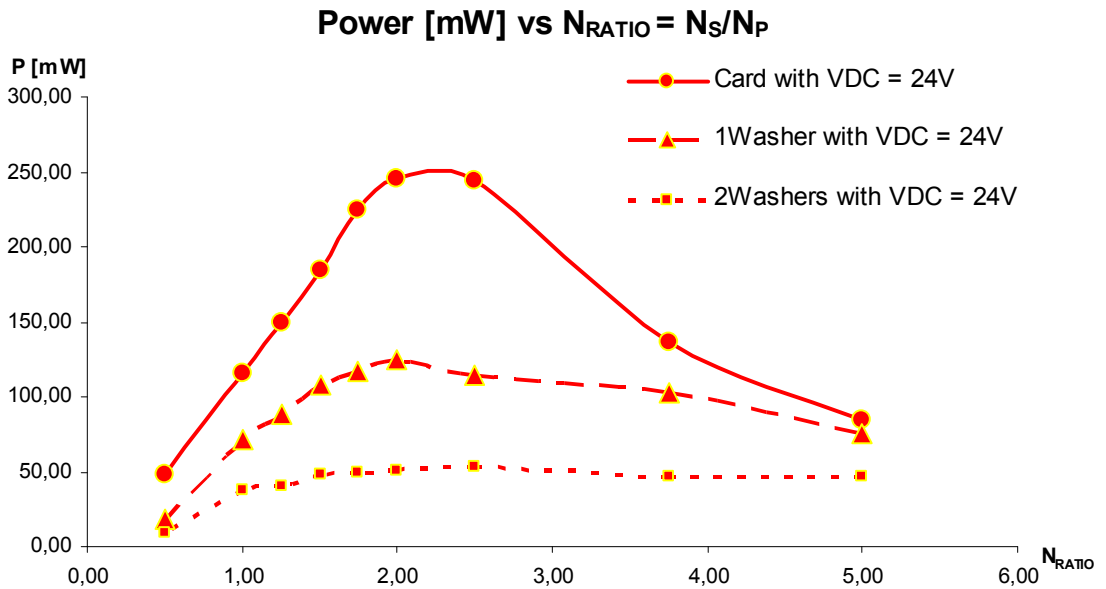

Figure 97: Comparative among data collected in different tests with the same V_{DC} = 24V